

ABSTRACT

JITTER FREQUENCY DETERMINING SYSTEM

A jitter frequency determining system is provided that includes a comparator, a clock source, a latching circuit, a memory device and a processor. The comparator is adapted to receive at least one output signal from a device under test and compare the output signal to an expected signal. The output signal has a repeating pattern. The clock source is adapted to produce a sampling clock based on user inputs, wherein the user inputs comprise a number of bits per one period of the repeating pattern, a length of a single bit period, a target effective sampling resolution and a number of times to sweep the repeating pattern. The clock source is further adapted to change the time between locally-in-order strobes to adjust the measurement bandwidth. The latching circuit is adapted to obtain samples of the output signal according to the sampling clock. The memory device is adapted to store the sampled data. The processor is adapted to analyze the stored data to determine jitter and to express jitter as a function of frequency.

Figure 5