CLAIMS

1. A chip comprising

a substrate having a first surface and a second surface opposite the first surface;

an integrated circuit mounted on a landing zone on the first surface of the substrate, the landing zone defining a landing zone region of the substrate being surrounded by a peripheral region of the substrate;

a plurality of contacts provided about the first surface in the peripheral region;

a plurality of wire-bonds providing electrical connections between the integrated circuit and the plurality of contacts;

a plurality of solder ball connections provided in the peripheral region on the second surface;

a plurality of connections provided in the substrate for connecting the electrical contacts on the first surface with the solder ball connections on the second surface;

characterized in that the substrate comprises at least one conductive track routed through the landing zone region of the substrate, wherein the chip is configured such that an alteration in the at least one conductive track prevents operation of the integrated circuit; and

the at least one conductive track is a security track forming part of a security mechanism, wherein the security mechanism is configured to detect an interference with the integrity of the security track and in response to enable at least one counter measure;

characterized in that the security mechanism comprises: a signal transmitter on the integrated circuit for providing a signal to a first end of the security track; and

a detection circuit connected to a second end of the security track for detecting an alteration to the signal;

wherein the security mechanism further comprises a response circuit responsive to the detection circuit for causing the performance of the at least

one counter measure and wherein the at least one countermeasure comprises resetting or disabling all or part of functionalities of the chip.

2. A chip according to claim 1, wherein a ground plane is provided as a layer of conductive material in the region of the substrate and wherein the at least one track follows an isolated path partitioning the ground plane.

3. A chip according to claim 1, wherein a power plane is provided as a layer of conductive material in the landing zone region of the substrate and the at least one track follows an isolated path partitioning the power plane.

4. A chip according to claim 1, wherein the at least one conductive track is electrically connected to at least one solder ball, wherein the at least one solder ball is positioned in the landing zone region of the substrate.

5. A chip according to any preceding claim, wherein the at least one conductive track provides an electrical connection to the integrated circuit which is required for the normal operation of the integrated circuit.

6. A method for protecting a wire-bond packaged ball grid array chip against alterations, comprising the steps of

forming a substrate having a first surface and a second surface opposite the first surface having a landing zone for an integrated circuit, the landing zone defining a landing zone region of the substrate, the forming of the substrate including providing a plurality of contacts about the first surface in a peripheral region, the peripheral region surrounding the landing zone region;

mounting the integrated circuit on the landing zone;

connecting a plurality of wire-bonds between the integrated circuit and the plurality of contacts;

providing a plurality of solder ball connections on a peripheral region of the second surface;

wherein the step of forming the substrate include providing a plurality of connections in the substrate for connecting the electrical contacts on the first surface with the solder ball connections on the second surface;

characterized in that the forming of the substrate comprises routing at least one conductive track through the landing zone region of the substrate, wherein the chip is configured such that an alteration in the at least one conductive track prevents operation of the integrated circuit; and

the at least one conductive track is a security track, the method further comprises providing a security mechanism including the security track, wherein the security mechanism is configured to detect an interference with the integrity of the security track and in response to enable at least one counter measure;

characterized in that the security mechanism provides a signal to a first end of the security track; and

detecting an alteration to the signal at a second end of the security track and in response to detecting an alteration causing the performance of the at least one counter measure and wherein the at least one countermeasure comprises resetting or disabling all or part of the functions of the chip.

7. A method according to claim 6, wherein the method comprises the step of forming a layer of conductive material in the landing zone region of the substrate to act as a ground plane wherein the at least one track follows an isolated path partitioning the ground plane.

8. A method according to claim 7, further comprising providing a layer of conductive material in the landing zone region of the substrate to act as a power plane and the at least one track follows an isolated path partitioning the power plane.

9. A method according to claim 7, further comprising the step of forming a conductive path using the at least one conductive track between one of the contacts of the first surface and at least one solder ball, wherein the at least one solder ball is positioned in the landing zone region of the substrate.

10. A method according to any one of claims 6 to 9, wherein the at least one track provides an electrical connection to the integrated circuit which is required for the subsequent correct operation of the integrated circuit.