

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
27 November 2003 (27.11.2003)

PCT

(10) International Publication Number
WO 03/098633 A2

(51) International Patent Classification⁷:	G11C
(21) International Application Number:	PCT/US03/15589
(22) International Filing Date:	15 May 2003 (15.05.2003)
(25) Filing Language:	English
(26) Publication Language:	English
(30) Priority Data:	
10/146,154	15 May 2002 (15.05.2002) US
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(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GO, GW, ML, MR, NE, SN, TD, TG).

Published:

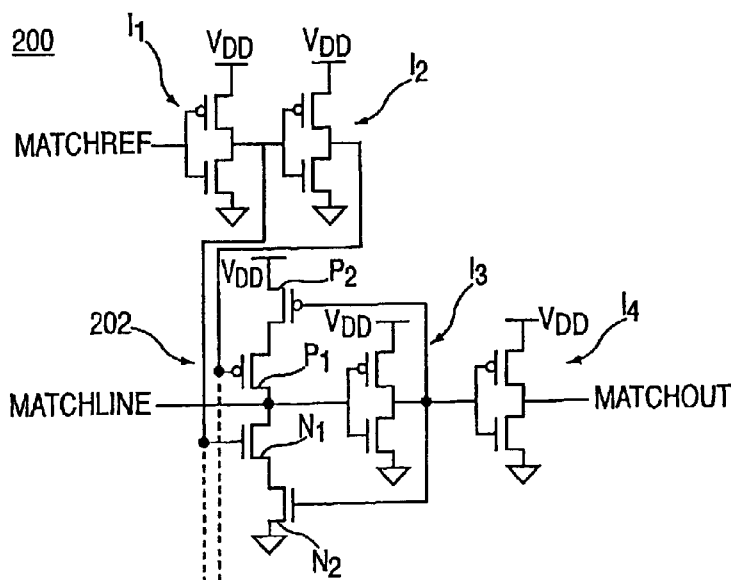
— *without international search report and to be republished upon receipt of that report*

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(54) Title: CONTENT ADDRESSABLE MEMORY (CAM) WITH ERROR CHECKING AND CORRECTION



(57) Abstract: A content addressable memory (CAM) (100) capable of ignoring and correcting bit errors contained therein is disclosed. In an exemplary embodiment, the CAM includes a plurality of individual CAM cells (102) for storing a codeword having a number of bits associated therewith. A match line (MATCHLINE) is coupled to each of the plurality of individual CAM cells, and is used to indicate a match status of a comparand word (104) that is compared to the stored codeword. The match status is reflective of either a match state or a mismatch state. A sensing apparatus (200) is used for latching the match line to the match state whenever the comparand word (104) mismatches the stored codeword by a number of N or fewer bits, wherein N is defined a maximum number of correctable bits for a given error checking and correction (ECC) algorithm used.