Electron Device Lett., vol.25, No.7, pp.459-461, Jul 2004.

[Non-patent document 3] Toshihide Kikkawa et al. "Highly Uniform AlGaN/GaN Power HEMT on a 3-inch Conductive N-SiC Substrate for Wireless Base Station Application", Technical Digest of IEEE CSIC 2005 Symposium, vol.25, No.7, pp.77-80.

SUMMARY ~~OF THE INVENTION~~

[0021]

However, the structures shown in FIGS. 23 and 24 have the problem of poor quality.

[0022]

According to the HEMT 1020 shown in FIG. 23, an insulating Fz-Si substrate 1061 is used as the substrate. The elastic limit of Fz-Si substrate 1061 is low. For this reason, during the growth of the nitride buffer layer 1052, the stress received from the nitride buffer layer 1052 due to the difference in the lattice constant values between the Fz-Si substrate 1061 and the nitride buffer layer 1052 made the substrate susceptible to plastic deformation. As a result, there was a problem that the warpage of the substrate increased to an inappropriate level in the HEMT manufacturing process. In addition, since Si has a smaller band gap than SiC, the resistance tends to be low at under high temperatures. For this reason, when the temperature of the substrate rises due to the amplification operation of the HEMT, the resistance of Si contained in the substrate is easily lowered, resulting in significant loss of high frequency signals.

[0023]

The HEMT 1030 shown in FIG. 24 uses an n-type SiC substrate 1062 as the substrate. The conductivity of this n-type SiC substrate 1062 is high. For this reason, it was necessary to thicken the nitride buffer layer 1052 in order to construct the area around the two dimensional electron gas 1053a with a highly insulating material. When the nitride buffer layer 1052 is thickened, there are problems that cracks are likely to occur in the nitride buffer layer 1052 and the warpage of the substrate increases. In addition, from the viewpoint of manufacturing cost, the merit of replacing the semi-insulating SiC substrate with the n-type SiC substrate is offset by the demerit of forming a thick nitride buffer layer. For this reason, in terms of manufacturing cost, the HEMT 1030 shown in FIG. 24 was no better than the HEMT 1010 shown in FIG. 22.

[0024]

The present invention is to solve the above problems, and the object is to provide a compound semiconductor substrate and a compound semiconductor device of high quality.

[0025]

According to one aspect of the present ~~invention~~disclosure, a compound semiconductor substrate comprises: a Si substrate with O concentration of $3*10^{17}/cm^3$ or more and $3*10^{18}/cm^3$ or less, a SiC layer formed on the Si substrate, a first nitride semiconductor layer made of $Al_xGa_{1-x}N$ ($0.1 \leqq x \leqq 1$), formed on the SiC layer and including an insulating or semi-insulating layer, a second nitride semiconductor layer formed on the first nitride semiconductor layer and including a main layer comprising of insulating or semi-insulating $Al_yGa_{1-y}N$ ($0 \leqq y < 0.1$), an electronic traveling layer formed on the second nitride semiconductor layer and made of $Al_zGa_{1-z}N$ ($0 \leqq z < 0.1$), and a barrier layer formed on the electronic traveling layer and having a wider band gap than a band gap of the electronic traveling layer, wherein a sum total thickness of the first and second nitride semiconductor layers and the electronic traveling layer is 6 micrometers or more and 10 micrometers or less.

includes both the first region and the second region, and a distance between the first region and the SiC layer is less than a distance between the second region and the SiC layer.

[0033]

Preferably, according to the compound semiconductor substrate, the first nitride semiconductor layer has a thickness less than or equal to a thickness of the second nitride semiconductor layer.

[0034]

Preferably, according to the compound semiconductor substrate, the electronic traveling layer has a thickness of 0.3micrometers or more.

[0035]

Preferably, according to the compound semiconductor substrate, stipulating a least squares plane of a top surface of the compound semiconductor substrate, when a sum total value of distance from the least squares plane to a highest point of the top surface of the compound semiconductor substrate and distance from the least squares plane to a lowest point of the top surface of the compound semiconductor substrate is defined as a warpage amount, the warpage amount is 0 or more and 50 or less micrometers.

[0036]

Preferably, according to the compound semiconductor substrate, regions other than an area where a distance from an outer edge of a top surface of the compound semiconductor substrate is 5 millimeters or less do not contain cracks.

[0037]

Preferably, according to the compound semiconductor substrate, the compound semiconductor substrate has a disk shape and a diameter of 100 millimeters or more and 200 millimeters or less.

[0038]

Preferably, according to the compound semiconductor substrate, a top surface of the compound semiconductor substrate does not contain traces of meltback etching.

[0039]

According to another aspect of the present ~~invention~~disclosure, a compound semiconductor substrate comprises: a conductive SiC substrate with resistivity of 0.1 Ωcm or more and less than $1*10^5$ Ωcm, a first nitride semiconductor layer made of $Al_xGa_{1-x}N$ ($0.1 \leqq x \leqq 1$), formed on the SiC layer and including an insulating or semi-insulating layer, a second nitride semiconductor layer formed on the first nitride semiconductor layer and containing a main layer comprising of insulating or semi-insulating $Al_yGa_{1-y}N$ ($0 \leqq y < 0.1$), an electronic traveling layer formed on the second nitride semiconductor layer and made of $Al_zGa_{1-z}N$ ($0 \leqq z < 0.1$), and a barrier layer formed on the electronic traveling layer and having a wider band gap than a band gap of the electronic traveling layer, wherein a sum total thickness of the first and second nitride semiconductor layers and the electronic traveling layer is 6 micrometers or more and 10 micrometers or less, the second nitride semiconductor layer further includes one or more intermediate layer formed at least one of inside the main layer and on the main layer, the intermediate layer comprising of $Al_yGa_{1-y}N$ ($0.5 \leqq y \leqq 1$), and the main layer has at least one of C concentration higher than that of the electronic traveling layer and Fe concentration higher than that of the electronic traveling layer.

[0040]

According to another aspect of the present ~~invention~~disclosure, a compound semiconductor device comprises: the compound semiconductor substrate above mentioned, first and second electrodes formed on the barrier layer, and a