

FLASH MEMORY CELL ON SeOI HAVING A SECOND CONTROL GATE
BURIED UNDER THE INSULATING LAYER

DESCRIPTIVE ABSTRACT

The invention relates, according to a first aspect, to a flash memory cell (1, 10) consisting of an FET transistor with a floating gate (10, 20) on a semiconductor on insulator substrate comprising a thin film of semiconductor material separated from a base substrate (5) by an insulating (BOX) layer, the transistor having, in the thin film, a channel (4), characterized in that it comprises two control gates, a front control gate (12, 22) being arranged above the floating gate (10, 20) and separated therefrom by an inter-gate dielectric (13, 23) and a back control gate (6, 34-37) being arranged within the base substrate (5) directly under the insulating (BOX) layer so as to be separated from the channel (4) only by the insulating (BOX) layer, the two control gates (10, 20; 6, 34-37) being designed to be used in combination to perform a cell programming operation. The invention also extends to a memory array comprising a plurality of memory cells according to the first aspect of the invention, and to a method of fabricating such a memory cell.

FIGURE 2