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(54) Title: CLOCK GENERATION CIRCUIT**(57) Abstract**

A clock generation circuit of the present invention extracts a phase error signal of a digital signal obtained from a recording medium (1) by a phase comparator (4), filters the phase error signal by a loop filter (5), converts the signal into an analog signal by a minute control D/A converter (6), detects whether the signal is within a set range by a range detector (9), generates a modulation reference signal by a modulation reference signal generator (10), modulates the modulation reference signal by a pulse width modulator (11), adds a frequency set value and the modulation reference signal by an adder (12), converts the addition result into an analog signal by a rough control D/A converter (13), cuts high-band components of the analog signal by a low-pass filter (14), adds the analog signals output from the minute control D/A converter (6) and the low-pass filter (14) by an analog adder (7), and outputs a clock signal by a voltage controlled oscillator (8) on the basis of an output signal of the analog adder (7). Thereby, a clock signal which can continuously lock a wide frequency range can be generated.

