A PROGRESSIVE TRIMMING METHOD

Field of the invention and prior art

The present invention relates to the field of producing multilayer semiconductor structures or substrates (also termed multilayer semiconductor wafers) produced by transfer of at least one layer onto a support. The transferred layer is formed by molecular bonding of a first wafer onto a second wafer or support, the first wafer generally being thinned following bonding. The first wafer may also include all or part of a component or a plurality of microcomponents, as happens with three-dimensional (3D) integration of components, which requires transfer of one or more layers of microcomponents onto a final support, and also as happens with circuit transfer as, for example, in the fabrication of back lit imaging devices.

The edges of the wafers used to form the transferred layers and the supports generally have chamfers or edge roundings serving to facilitate their manipulation and to avoid breakages at the edges that could occur if those edges were to project, such breakages being sources of particles that contaminate the wafer surfaces. The chamfers may be rounded and/or bevelled in shape.

However, the presence of such chamfers prevents good contact between the support and the wafer at their peripheries. As a result, a peripheral zone exists on which the transferred layer is not bonded or not properly bonded to the support substrate. This peripheral zone of the transferred layer must be eliminated since it is liable to break in an uncontrolled manner and contaminate the structure with unwanted fragments or particles.

Thus, once the wafer has been bonded to the support and after any necessary thinning thereof, the transferred layer is then trimmed in order to remove the peripheral zone over which the chamfers extend. Trimming is usually carried out essentially by mechanical machining, in

particular by abrasion or grinding from the exposed surface of the transferred layer up to the support.

However, such trimming causes problems with peel-off, both at the bonding interface between the transferred layer and the support and in the transferred layer itself. More precisely, at the bonding interface, peel-off problems correspond to delamination of the transferred layer over certain zones in the vicinity of the periphery of the layer, which delamination may be qualified as macro peel-off. The bonding energy is lower near the periphery of the layer because of the presence of the chamfers. As a consequence, grinding in this region may cause partial detachment of the layer at its bonding interface with the support substrate. Said detachment is more probable when the transferred layer includes components. High temperature anneals, normally carried out after bonding to reinforce the bonding interface, are not used when components are present in the transferred layer since components cannot withstand the temperatures of such anneals.

Further, when the layer comprises components such as circuits, contacts, and in particular zones formed from metal, grinding may cause delamination at the motifs of the components present in the transferred layer, which delamination may be qualified as micro peel-off.

Such phenomena of macro and micro peel-off occur beyond a certain level of heating and/or mechanical stress in the structure during the trimming step. This level is frequently attained during complete trimming of the transferred layer.

Summary of the invention

The aim of the invention is to overcome the disadvantages mentioned above by proposing a method of trimming a structure comprising a first wafer bonded to a second wafer, the first wafer having a chamfered edge, the method comprising:

• a first trimming step carried out over a first depth comprising the thickness of the first wafer, said first trimming step also being carried out over a first predetermined width from the edge of the first wafer; and

• at least one second trimming step carried out over a second depth comprising at least the thickness of the first wafer, said second trimming step also being carried out over a second width that is less than the first width.

Thus, by carrying out a first trimming step as close as possible to the edge of the first wafer and over a predetermined width, the first wafer is attacked while remaining relatively far away from the components thereof. This limits heating and/or stresses in the structure even when trimming is intense, i.e. penetrating significantly into the second wafer.

Further, the heating and/or stresses are also limited during the second trimming step, even though said second trimming step is carried out at a distance that is further from the edge of the first wafer, i.e. close to the components. In fact, the material to be removed during the second trimming step is reduced because of the portion that has already been removed during the first trimming step.

As a result, the two trimming steps of the method of the invention mean that complete trimming of at least the first wafer can be carried out while substantially reducing the phenomena of macro and micro peel-off that normally appear during single-step trimming.

In accordance with one aspect of the invention, the second trimming step is carried out over a second depth that is less than or equal to the first depth over which the first trimming step is carried out.

In accordance with another aspect of the invention, the portion of the thickness of the second step withdrawn during the first trimming step is in the range 10 μm [micrometer] to 30 μm.

In accordance with another aspect of the invention, the portion of the thickness of the second wafer withdrawn during the second trimming step is in the range 0 to 10 μm.

In accordance with yet another aspect of the invention, the first trimming step is carried out over a first width in the range 2 mm [millimeter] to 10 mm, preferably in the range 2 mm to 6 mm, while the second trimming step is carried out over a second width in the range 0.1 mm to 2 mm.

The present invention also provides a method of producing a three-dimensional composite structure comprising at least one step of producing a layer of components on one face of a first wafer, a step of bonding the face of the first wafer comprising the layer of components onto a second wafer, and a step of trimming at least the first wafer carried out in accordance with the trimming method of the invention.

The use of the trimming method of the invention means that three-dimensional structures can be produced by stacking two or more wafers, minimizing the risks of delamination both at the bonding interfaces between the wafers and at the component layers. One of the component layers may include image sensors.

Brief description of the figures

- Figure 1 is a top view of a structure to be trimmed;
- Figures 2A to 2E are diagrammatic views of a trimming method in accordance with one implementation of the invention;
- Figure 3 is a flow diagram of the steps carried out during the method illustrated in Figures 2A to 2E;
- Figures 4A to 4F are diagrammatic views showing the production of a three-dimensional structure employing the trimming method of the present invention;

• Figure 5 is a flow diagram of the steps carried out during production of the three-dimensional structure illustrated in Figures 4A to 4F;

• Figure 6 is a view showing the lower surface of the grinder used in Figures 4D and 4E.

Detailed description of implementations of the invention

The present invention is of general application to trimming a structure comprising at least two wafers assembled together by molecular bonding or any other type of bonding such as anodic bonding, metallic bonding, or bonding with adhesive, it being possible for components to be formed beforehand in the first wafer that is then bonded to the second wafer that constitutes a support. The wafers are generally of circular outline, possibly with different diameters, in particular diameters of 100 millimeters (mm), 200 mm, or 300 mm. The term "components" as used here means any type of element produced with materials that differ from the material of the wafer and that are sensitive to the high temperatures normally used to reinforce the bonding interface. These components correspond in particular to elements forming all or a portion of an electronic component or a plurality of electronic microcomponents, such as circuits or contacts or active layers that may be damaged or even destroyed if they are exposed to high temperatures. The components may also correspond to elements, motifs, or layers that are produced with materials with expansion coefficients different from that of the wafer and that, at high temperature, are liable to create different degrees of expansion in the wafer, which may deform and/or damage it.

In other words, when the first wafer include such components, it cannot undergo high temperature anneals after bonding. As a consequence, the bonding energy between the wafers is limited, which renders the resulting structure rather more sensitive to the

phenomenon of macro peel-off during mechanical trimming, as described above. Further, as explained above, the trimming may also cause micro peel-off, corresponding to delamination in the first wafer at the components (detachment in one or more of the stacks forming the components in the first wafer).

More generally, the invention is of particular application to assembled structures that cannot be subjected to a high temperature bonding anneal, as also applies with heterostructures formed by an assembly of wafers with different expansion coefficients (for example silicon-on-sapphire, silicon-on-glass, etc). It may also apply to more standard silicon-on-insulator (SOI) type structures, namely SOI structures in which the two wafers are composed of silicon. For this type of structure, the invention is of particular application to the formation of structures that have a layer thickness of more than 10 micrometers (μm), or that comprise a stack of layers of different natures. In fact, it has been observed that these structures are liable to be damaged during the trimming step when said trimming is carried out using the known prior art technique.

To this end, the present invention proposes carrying out progressive trimming from the edge of the first wafer. More precisely, as explained below in more detail, the trimming method of the invention is carried out in at least two steps, namely a first trimming step carried out as close as possible to the edge of the wafer and a second trimming step carried out at a distance further from the edge of the first wafer, i.e. over a portion that is closer to the components of the wafer.

Figure 1 is a top view showing a structure 15 comprising a wafer 10 bonded to a subjacent support (not shown). The wafer 10 includes components 11 formed in a zone 14 termed the "useful zone" that covers the major portion of the surface of the wafer with the exception of an annular exclusion portion with a width ℓ_3 corresponding

to the distance between the edge 10a of the wafer 10 and the frontier of the useful zone 14. The annular exclusion portion comprises at least the zone over which the chamfers of the wafer extend. This annular portion may be divided into first and second annular zones 12 and 13. The first annular zone 12 with width ℓ_1 is the zone that is closest to the edge 10a of the wafer. It is on this first zone 12 that the first trimming step of the method of the invention is carried out. This first zone is relatively distanced from the useful zone 14 including the components 11, and so trimming may be carried out in the structure without running the risk of macro or micro peel-offs. The second annular zone 13 with width ℓ_2 that is less than the width ℓ_1 is further from the edge 10a of the wafer, i.e. closer to the useful zone 14. However, since a large quantity of material has already been withdrawn during the first trimming step, heating and stresses are limited during the second step of trimming of the second annular zone 13. Thus, any macro and/or micro peel-off phenomena that could occur during trimming are limited.

During the second trimming step, heating and stresses may be further reduced by carrying out trimming over a depth that is less than the depth over which the first trimming step is carried out.

In order to further limit heating and stresses during trimming, the method of the invention may also be carried out in more than two steps, for example three or four trimming steps. Under such circumstances, each of the successive trimming steps is carried out over a width that is less than or identical to that of the preceding trimming step. The trimming depth for each step is preferably but not exclusively smaller than that of the preceding trimming step.

One implementation of a trimming method is described below with reference to Figures 2A to 2E and 3.

As can be seen in Figure 2A, a structure 100 to be trimmed is formed by assembling a first wafer 101 of the same type as that of Figure 1 with a second wafer 102, for example formed from silicon. The first and second wafers 101 and 102 have the same diameter here. They could, however, have different diameters. In the example described here, assembly is carried out using the molecular bonding technique that is well known to the skilled person. It should be recalled that the principle of molecular bonding is based on bringing two surfaces into direct contact, i.e. without using a specific bonding material (adhesive, wax, solder etc). Such an operation requires that the surfaces to be bonded are sufficiently smooth, free from particles or contamination, and that they are brought sufficiently close together to allow contact to be initiated, typically to a distance of less than a few nanometers. Under such circumstances, forces of attraction between the two surfaces are high enough to cause molecular bonding (bonding induced by the set of attractive forces (van der Waals forces) due to electrons interacting between atoms or molecules of the two surfaces to be bonded together).

Adhesion between the two wafers is carried out at a low temperature so as not to damage the components and/or the first wafer. More precisely, after bringing the wafers into contact at ambient temperature, a bonding reinforcement anneal may be carried out, but at a temperature of less than 450°C, beyond which temperature certain metals such as aluminum or copper begin to creep.

A bonding layer 107 of the oxide layer type is formed on the bonding face of the first wafer 101 and/or on the second wafer before bringing it into contact with the second wafer 102. The first wafer 101 comprises a layer of components 103 and has a chamfered edge, i.e. an edge comprising an upper chamfer 104 and a lower chamfer 105. In Figure 2A, the wafers have rounded chamfers.

However, the wafers may also have chamfers or edge roundings with different shapes such as in the form of a bevel. In general, the term "chamfered edge" means any wafer edge at which the ridges have been bevelled so that contact between the two wafers close to their periphery is poor.

The wafers 101 and 102 are assembled one against the other by molecular bonding to form the structure 100 (step S1, Figure 2B). Depending on the initial thickness of the first wafer 101, this may be thinned in order to form a transferred layer 106 with a predetermined thickness e_1 (step S2, Figure 2C), for example approximately 10 µm. The thickness e_1 is measured between the upper face and the lower face of the layer or the wafer beyond the chamfered edge. This thinning step is preferably carried out before the trimming operation. Thinning of the first wafer, however, is still optional and trimming of the first wafer may be carried out without carrying out a prior thinning step.

Next, trimming of the structure 100 is carried out, principally consisting in eliminating an annular portion of the layer 106 comprising the chamfer 105, the chamfer 104 having been eliminated during thinning of the first wafer 101. In accordance with the invention, trimming commences with a first trimming step carried out over a width ld_1 from the edge of the first layer 106 that corresponds to the edge of the first wafer 101 (step S3, Figure 2D). For wafers with a diameter of 100 mm, 200 mm and 300 mm, the trimming width ld_1 is generally in the range 2 mm to 10 mm, preferably in the range 2 mm to 6 mm. Trimming is carried out by action or mechanical machining from the upper face of the layer 106 (edge grinding). The mechanical action may be exerted using a grinder or any other tool that is capable of mechanically wearing away the material of the layer.

During said first trimming step, the structure 100 is attacked over a depth Pd_1, defined from a reference

plane corresponding to the bonding interface (in this instance the plane of contact between the bonding layer 107 and the bonding face of the second wafer 102). The depth Pd_1 comprises the thickness e_1 of the layer 106, the thickness e_2 of the bonding layer 107 and a thickness e_3 corresponding to a portion of the thickness of the second wafer 102. The thickness e_3 is in the range 10 µm to 30 µm. In Figure 2D, the flank of the trimmed layer 106 is shown in a diagrammatic manner as being perpendicular to the plane of the substrate. However, depending on the type of grinder used, the profile of the trimming flank may have different shapes that are not entirely rectilinear, such as a slightly inwardly curved shape. In particular, such inwardly curved flanks are obtained when the grinder or trimming wheel is provided with grooves over at least one of these faces. It appears that the presence of such grooves encourages evacuation of the eliminated material and circulation of liquid (generally water) dispensed over and close to the wheel during the trimming operation. This further limits heating/stresses at the wafer edge and can further improve the trimming quality. In circumstances where the trimmed flank of the layer or wafer does not have a near rectilinear profile, the widths of the trimming steps (such as widths ld_1 and ld_2) correspond at least to the widths with which the wafer or layer is attacked (the trimming width can then be slightly reduced during trimming).

Trimming is then completed by a second trimming step that is also carried out by mechanical action or machining (step S4, Figure 2E). This second trimming step is carried out from a predetermined distance from the edge of the layer 106 corresponding to the trimming width ld_1 of the first step. For wafers with a diameter of 100 mm, 200 mm, and 300 mm, the trimming width ld_2 is generally in the range 0.1 mm to 0.2 mm.

In this second trimming step, the structure 100 is attacked over a depth Pd_2 comprising at least the thickness e_1 of the layer 106. The depth Pd_2 may also comprise a thickness e_4 corresponding to a portion of the thickness of the second wafer 102. In the example described here, the thickness e_4 is less than the thickness e_3. It is in the range 0 to 10 µm, for example 5 µm. As indicated above, the thickness e_4 may also be greater than or equal to the thickness e_3.

A particular but not exclusive field for the trimming method of the present invention is that of producing three-dimensional structures.

A method of producing a three-dimensional structure by transfer onto a support of a layer of microcomponents formed on an initial substrate in accordance with an implementation of the invention is described below in relation to Figures 4A to 4G and 5.

Producing the three-dimensional structure starts with the formation of a first series of microcomponents 204 on the surface of a first wafer 200 the edge of which has an upper chamfer 206 and a lower chamfer 205 (Figure 4A, step S1). In the example described here, the first wafer 200 is a multilayer SOI type structure, i.e. it comprises a layer of silicon 201 disposed on a substrate 203, also of silicon, a buried oxide layer 202 (for example a layer of SiO_2) being present between the layer 201 and the substrate 203. The wafer 200 has a thickness in the range approximately 600 µm to 900 µm. For a wafer 200 mm in diameter (8 inches), the standard thickness is 725 µm.

The microcomponents 204 are formed by photolithography using a mask that can define zones for the formation of motifs corresponding to the microcomponents to be produced.

The face of the first wafer 200 comprising the microcomponents 204 is then brought into intimate contact with a face of a second wafer 300 (step S2, Figure 4B)

with a view to bonding by molecular bonding. The wafer 300 has a thickness of approximately 725 µm. In the same manner as the first wafer 200, the edge of the second wafer 300 has an upper chamfer 301 and a lower chamfer 302. A layer of oxide 207, for example formed from SiO_2, is also formed on the face of the first wafer 200 comprising the microcomponents 204. In the example described here, the first and second wafers 200, 300 have a diameter of 200 mm.

After bonding, and as can be seen in Figure 4C, the first wafer 200 is thinned to withdraw a portion thereof present above the layer of microcomponents 204 (step S3), here the substrate 203. At this stage of the method, the buried layer 202 is preferably retained in order to protect the components from possible contamination, particles, etc. The first wafer 200 may be thinned, in particular by a step of grinding or chemical-mechanical polishing (CMP) of the substrate 203, stopping 50 µm from the bonding interface, followed by a step of chemical attack up to the buried oxide layer 202, for example by etching with tetramethylammonium hydroxide (TMAH). Thinning may also be carried out by cleavage or fracture along a plane of weakness previously formed in the wafer 200 by atomic implantation. Advantageously, the buried insulating layer 202 is used to define the thickness of the remaining wafer 200. After the thinning step, the wafer 200 has a thickness e of approximately 10 µm. In other circumstances, its thickness may lie in the range 1 µm to 15 µm.

Thus, a composite structure 500 is obtained, formed by the second wafer 300 and the layer 201 corresponding to the remaining portion of the first wafer 200.

In accordance with the invention, the first step of mechanical trimming of the structure 500 is carried out, consisting of eliminating an annular portion of the wafer 200 (step S4, Figure 4D). This first trimming step is carried out using a grinder 400, the structure 500 being

held in a rotating plate (not shown). As can be seen in Figure 6, the grinder 400 has a lower face that is structured due to the presence of grooves 410. As indicated above, it has been observed that a grinder with such a structured face can limit heating and stresses. Clearly, trimming may also be carried out with grinders that do not have such structured faces.

During this first trimming step, the structure 500 is attacked over a width ld_1 in the range 2 mm to 10 mm and over a depth Pd_1 comprising the thickness e_1 of the remaining portion of the first wafer 200, the thickness e_2 of the oxide layer 207 and a thickness e_3 corresponding to a portion of the thickness of the second wafer 300, said thickness e_3 being in the range 10 µm to 30 µm.

Trimming is then completed by the second trimming step carried out from a predetermined distance from the edge of the wafer 200 corresponding to the trimming width ld_1 of the first step and over a width ld_2 in the range 0.1 mm to 2 mm (step S5, Figure 4E). In this second trimming step, the structure 500 is attacked over a depth Pd_2 comprising the thickness e_1 of the remaining portion of the first wafer 200, the thickness e_2 of the oxide layer 207 and a thickness e_4 corresponding to a portion of the thickness of the second wafer 300 in the range 0 to 10 µm, for example 5 µm.

Once trimming of the structure 500 has been terminated, after having withdrawn the layer 202, a second layer of microcomponents 214 is formed at the exposed surface of the layer 201 (Figure 4F, step S6). In the example described here, the microcomponents 214 are formed in alignment with the buried microcomponents 204. A photolithography mask is used for this purpose; it is similar to that used to form the microcomponents 204.

In a variation, the three-dimensional structure is formed by a stack of layers, i.e. by transfer of one or more additional layers onto the layer 201, each

additional layer being in alignment with the directly adjacent layer or layers. Each additional layer is trimmed progressively using the trimming method of the invention. Further, before each transfer of an additional layer, it is possible to deposit a layer of oxide on the exposed layer, for example a layer of tetraethyloxysilane (TEOS) oxide, in order to facilitate assembly and protect the trimmed zones(for which the material of the subjacent wafer is exposed) from subsequent chemical attacks. Alternatively, a single trimming operation may be carried out after the set of layers has been transferred. The thicknesses $\underline{e}_1$ and $\underline{e}_2$ of the materials eliminated during the trimming step of the invention then correspond to the thicknesses included between the upper surface of the upper layer of the stack and the stop interface for the trimming step at or within the support wafer.

In accordance with a particular implementation, one of the layers of microcomponents may in particular comprise image sensors.

In accordance with another implementation, the components have already been formed in the second support wafer before assembly thereof with the first wafer constituting the transferred layer.

In accordance with yet another implementation, the trimming steps may include a first rough removal step, for example using a grinder as represented in Figure 4D, followed by a finer removal step, for example using a wafer edge polish tool. This means that, after trimming, a wafer edge with reduced roughness can be produced that is less susceptible of having residual particles.

CLAIMS

1. A method of trimming a structure (100) comprising a first wafer (101) bonded to a second wafer (102), the first wafer having a chamfered edge (104, 105);

characterized in that it comprises a first trimming step carried out over a first depth (Pd_1) comprising the thickness (e_1) of the first wafer (101), said first trimming step also being carried out over a first predetermined width (ld_1) from the edge of the first wafer (101); and

· at least one second trimming step carried out over a second depth (ld_2) comprising at least the thickness (e_1) of the first wafer (101), said second trimming step also being carried out over a second width (ld_2) that is less than the first width (ld_1).

2. A method according to claim 1, characterized in that said second depth (Pd_2) is less than the first depth (Pd_1).

3. A method according to claim 1 or claim 2, characterized in that the portion of the thickness of the second wafer (102) withdrawn during the first trimming step is in the range 10 µm to 30 µm.

4. A method according to any one of claims 1 to 3, characterized in that the portion of the thickness of the second wafer (102) withdrawn during the second trimming step is in the range 0 to 10 µm.

5. A method according to any one of claims 1 to 4, characterized in that the first trimming step is carried out over a first width (ld_1) in the range 2 mm to 10 mm, preferably in the range 2 mm to 6 mm.

6. A method according to any one of claims 1 to 5, characterized in that the second trimming step is carried out over a second width (ld_2) in the range 0.1 mm to 2 mm.

7. A method according to any one of claims 1 to 6, characterized in that the first wafer (101) comprises components (103).

8. A method according to any one of claims 1 to 7, characterized in that at least one of the trimming steps is carried out with a grinder comprising grooves on its lower surface.

9. A method of producing a three-dimensional composite structure (500), comprising at least one step of producing a layer of components (204) on one face of a first wafer (200), a step of bonding the face of the first wafer (200) comprising the layer of components (204) onto a second wafer (300), and a step of trimming at least the first wafer (200) carried out in accordance with a trimming method in accordance with any one of claims 1 to 8.

10. A method according to claim 9, characterized in that it comprises, after the bonding step, a step of thinning the first wafer (200).

11. A method according to claim 9 or claim 10, characterized in that it further comprises a step of producing a second layer of microcomponents (214) on the face of the first wafer (200) opposite to the face comprising the first layer of components (204).

12. A method according to any one of claims 9 to 11, characterized in that it comprises, before the bonding step, a step of forming a layer of oxide (207) on the

face of the first wafer (200) comprising the first layer of components (204).

13. A method according to any one of claims 9 to 12, characterized in that the first wafer (200) is a SOI type structure.

14. A method according to any one of claims 9 to 13, characterized in that at least the first layer of components (204) comprises image sensors.