ABSTRACT

FOLDED BIT LINE DRAM WITH VERTICAL ULTRA THIN BODY TRANSISTORS

Methods describe forming a folded bit line DRAM device, which includes an array of memory cells, each with an outwardly extending pillar. Each pillar includes single crystalline first and second contact layers separated by an oxide layer. A single crystalline vertical transistor is formed along alternating sides of the pillar. The transistor includes an ultra thin single crystalline vertical: first source/drain region coupled to the first contact layer; second source/drain region coupled to the second contact layer; and body region that opposes the oxide layer and couples the first and the second source/drain regions. Buried bit lines formed of single crystalline semiconductor material are disposed below the pillars to interconnect the first contact layer of column adjacent pillars in the array of memory cells. Word lines are each disposed orthogonally to the bit lines, in a trench between rows of the pillars, for addressing alternating body regions of adjacent transistors.

Figure 3