

HIGH VOLTAGE DEVICE

ABSTRACT

A method of forming a device is disclosed. The method includes providing a substrate having a device region. The device region includes a source region, a gate region and a drain region defined thereon. The substrate is prepared with gate layers on the substrate. The gate layers are patterned to form a gate in the gate region and a field structure surrounding the drain region. A source and a drain are formed in the source region and drain region respectively. The drain is separated from the gate on a second side of the gate and the source is adjacent to a first side of the gate. An interconnection to the field structure is formed. The interconnection is coupled to a potential which distributes the electric field across the substrate between the second side of the gate and the drain.

Fig. 1a