

ABSTRACT

APPARATUS AND METHOD FOR INCREASED OPERAND AVAILABILITY IN A DATA PROCESSING UNIT WITH A STORE THROUGH CACHE MEMORY UNIT STRATEGY

In a data processing system in which each of the data processing units is implemented using pipeline techniques and has a cache memory unit employing a store through strategy, the time required to prepare a write instruction operand address can be substantially shorter than the time required by the execution unit to prepare the associated write instruction operand. In order to utilize time difference, apparatus is included in the execution (E-)cache unit for storing the write instruction operand address during the preparation of the associated write instruction operand. After storing the write instruction operand address, a next address is entered in an input register of the E-cache unit. When the newly entered address is associated with a read instruction, does not conflict with the write instruction operand address, and produces a "hit" signal when applied to the E-cache unit tag directory, the read instruction is processed by the E-cache unit. When a second write instruction operand address is entered in the input register, the read instruction operand address conflicts with the stored write instruction operand address or the read instruction operand address results in a "miss" when applied to the E-cache tag directory unit, the address is stored in the input register until the



write instruction operand has been determined and the associated write instruction has been processed by the E-cache unit.

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