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(54) IMPROVEMENTS IN OR RELATING TO INSULATED-GATE FIELD EFFECT TRANSISTORS

(71) We, NIPPON ELECTRIC COMPANY LIMITED, a Company duly organized and existing under the laws of Japan and having its executive office at 7-15, Shiba Gochome, Minato-ku, Tokyo-to, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to insulated-gate field effect transistors.

Generally, in a semiconductor integrated circuit, a high voltage resulting from static electricity, transient phenomena, etc., may be unexpectedly applied to the electrodes. This tends to cause the breakdown of the integrated circuits.

In an insulated gate field effect transistor, the insulator film under the gate electrode often suffers breakdown caused by such a high voltage. To avoid this breakdown, various protecting means have been proposed. For example, a diode is connected in parallel with the gate electrode of the insulated-gate field effect transistor whereby the gate insulator film is protected against an insulator breakdown resulting from the high voltage exceeding a certain value. This protection diode is formed in the substrate containing the insulated-gate field effect transistor. However the impurity concentration of the substrate cannot be made high enough to attain a favourable characteristic of the insulated gate field effect transistor. As a consequence, the breakdown voltage of the diode cannot be made lower than a value of the order of 100 V. This makes it difficult to realize a protection diode operable at a low breakdown voltage and to maintain sufficient protection effect for the field effect transistor. To make the diode breakdown voltage lower, a method has been proposed wherein an electrode is disposed on a comparatively thin insulation layer, above the PN junction, and the electrode is grounded, whereby the electric field on the surface of the PN junction is

concentrated and thus the breakdown voltage at the PN junction is lowered (Field induced junction).

According to this method, however, a large resistance is unavoidable at the breakdown point of the PN junction and it is difficult to obtain the desirable protection effect for the insulated gate field effect transistor.

An object of this invention is to provide a semiconductor device which is protected against breakdown of the gate insulator film resulting from a high voltage which may be applied to the gate electrode under operating conditions.

According to the present invention, there is provided an insulated gate field effect transistor with means for protecting the transistor against the application of a high input voltage to the gate thereof, comprising a semiconductor substrate of a first conductivity type, an insulated gate field effect transistor formed in said substrate and having source and drain regions and a gate electrode, said gate electrode being formed on an insulator film which is disposed on the substrate between said source and drain regions, a first region formed on said substrate at a location spaced from said transistor and being of a conductivity type opposite to said first conductivity type, the first region having an input terminal at one end thereof and an output terminal at the other end thereof and forming a resistor between the input and output terminals, and a second region formed on said substrate; said second region being in contact with said first region, being of the first conductivity type and having a high concentration of impurities, thereby to form with said first region a diode having a low breakdown voltage, wherein the output terminal of said first region is connected to said gate electrode, and the gate insulator film of said transistor is protected against breakdown by a high input voltage by said resistor and said diode.

In one embodiment of the invention the breakdown voltage at the PN junction be-

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tween the first and second regions can be set at a suitable value (80—20V) by arranging for the impurity concentration of the first region to have a suitable value, such as $5 \times 10^{15} \text{ cm}^{-3} \sim 5 \times 10^{16} \text{ cm}^{-3}$. The series resistance at the breakdown point is remarkably smaller than that in the field induced junction.

Furthermore, the voltage rise due to the series resistance produced in the event of breakdown at the PN junction is limited by the resistance component between the two ends of the first region, and thus the gate electrode of the insulated-gate field effect transistor connected to one end of the first region is protected from a high voltage unexpectedly applied to the other end of the first region.

In summary, the present embodiment has a protection diode operable at a low breakdown voltage and at a small series resistance appearing in the event of breakdown which is connected in parallel with a gate electrode. Therefore, even if a high voltage is applied to the signal input electrode, the voltage applied actually to the gate electrode of the field effect transistor can be limited to a sufficiently low value compared with that in the prior art.

The invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is an equivalent circuit diagram of a field effect transistor with protection mean according to this invention;

Figs. 2(a) and (b) illustrate a plan view and a cross sectional view of a first field effect transistor according to the invention, respectively;

Fig. 3 diagrammatically shows the reverse voltage—current characteristics of two PN junctions formed in a gate protection device in the embodiment shown in Fig. 2;

Fig. 4 is a diagram showing the relationship between input and output voltages in connection with the embodiment as in Fig. 2, and

Figs. 5(a) and (b) show a plan view and a cross-sectional view of another embodiment of this invention, respectively.

The transistors shown in the drawings each comprise a semiconductor substrate in which an insulated gate field effect transistor and first and second regions having high concentrations of impurities are formed. The first region is of the opposite conductivity type to that of the substrate, while the second region is of the same conductivity type as that of said substrate. The second region is in contact with one end of the first region, and the second region and/or the substrate is grounded. The end of the first region in contact with the second region is connected to the gate electrode of the insu-

lated gate field effect transistor, and the other end of the input electrode.

Referring to Figure 1, there is shown a circuit diagram of a transistor and gate protection device according to this invention. In this figure a gate protection device 200 is disposed immediately before the gate of an insulated gate field effect transistor 100 for the purpose of preventing insulation breakdown which may be caused when an abnormal voltage is applied to the gate.

Referring to Fig. 2, the semiconductor device comprises an N type silicon substrate 1 having an impurity concentration of about 10^{16} cm^{-3} ; an insulated gate field effect transistor 100 having a source region 11, drain region 12 and gate electrode 13; a gate protection device 200 having a P⁺ type region 3, N⁺ type region 2; an input terminal 5 and output terminal 6; and a wiring layer 14 electrically connecting the output terminal 6 to the gate electrode 13. The N⁺ type region 2 is formed in the substrate 1 by the known selective diffusion technique, and then the region 3, source region 11 and drain region 12, which are P⁺ type, are formed by a diffusion technique in the same way. The impurity concentration of the N⁺ type region 2 is about 10^{16} cm^{-3} , and that of the P⁺ type regions 3, 11 and 12 is about 10^{19} cm^{-3} . Finally, aluminum is evaporated on to both surfaces of the substrate 1, and then the input terminal 5, output terminal 6, wiring layer 14, source electrode 15, drain electrode 16, gate electrode 13 and ground electrode 8 are formed by the ordinary photo-etching technique.

In the above structure, the resistance component existing between the terminals 5 and 6 is about 3 k Ω , and the terminal 6 is located adjacent to the PN junction 22 formed between the N⁺ type region 2 and the P⁺ type region 3.

The terminal 5 is used as an input terminal, the terminal 6 as an output terminal which is connected to the gate electrode of the insulated gate field effect transistor 100, and the electrode 8 as an electrode connected to the ground circuit.

The foregoing structure can be easily formed by known semiconductor techniques and, hence, the forming process of the semiconductor device is not described in this specification.

In the above embodiment, the breakdown voltage at the PN junction 22 formed between the P⁺ type region 3 and the N⁺ type region 2 is about 40 V, and that at the PN junction 21 formed between the P⁺ type region 3 and the N type silicon substrate 1 is about 90 V.

The above semiconductor device is operated in the following manner. Referring to Figure 3, this shows the backward bias voltage vs current characteristics of the PN junctions 21 and 22, $I_{(A)}$ for that of the PN

junction 22, and $I_{(B)}$ for that of the PN junction 21.

Fig. 4 shows the relationship between the voltage applied to the input terminal 5 and the voltage applied to the output terminal 6 shown in Figure 2(a). It is assumed that an input voltage $V_{(a)}$ is applied to the input terminal 5. When the voltage $V_{(a)}$ at the input terminal 5 is increased, the voltage $V_{(b)}$ at the output terminal 6 is increased accordingly. When the voltage $V_{(b)}$ at the output terminal 6 exceeds the breakdown voltage BV_{j6} of the PN junction 22, a current corresponding to the characteristic shown in Figure 3 flows and the voltage $V_{(b)}$ at the output terminal 6 increases according to the following relationship.

$$V_{(b)} = BV_{j6} + \frac{r}{R+r} (V_{(a)} - BV_{j6})$$

where

R denotes the resistance value due to the P⁺ type layer 3 lying between input terminal 5 and output terminal 6, and r denotes the resistance of the PN junction between the N⁺ region 2 and the P⁺ layer 3 when the PN junction is in a state of breakdown.

In the above embodiment, R is 3 kΩ, r is 50 Ω, and BV_{j6} is 40 V. Hence the voltage $V_{(b)}$ at the output terminal 6 does not exceed BV_{j6} . For example, when $V_{(a)}$ is 1,000 V, $V_{(b)}$ is limited to 56 V.

When the voltage $V_{(a)}$ at the input terminal 5 exceeds the breakdown voltage BV_{j6} of the PN junction 21, a current corresponding to the characteristic $I_{(B)}$ shown in Figure 3 flows therein. The magnitude of this current is not appreciably large because the resistance component is large enough as shown in Figure 2 $I_{(B)}$.

Therefore, compared with the conventional devices, the semiconductor device of Figures 2(a) and 2(b) has the technical advantages that the breakdown voltage of the protection diode is low; the resistance component produced at the breakdown point is small; and there is no possibility of producing an abnormally high voltage even in the event of the diode breakdown. According to the prior art, it has been impossible to lower the breakdown voltage. Whereas, a sufficiently low breakdown voltage is obtained in the device of Figures 2(a) and 2(b) by controlling the impurity concentration of the N⁺ type region 2. This can be achieved in an insulated gate field effect transistor whose gate insulator film is thin.

In the prior art, the breakdown voltage can be reduced considerably by the use of field induced junction diode. On the other hand, however, the resistance component pro-

duced at the breakdown point is large, and a high voltage comes out at the output terminal in the event of diode breakdown. After all, the prior art is not sufficiently effective for the purpose of circuit protection. Whereas, in the device of Figures 2(a) and 2(b) the resistance component produced at the breakdown point is small, and there is no possibility of producing a high voltage at the output terminal by virtue of the resistance component of the P⁺ type region 3 even in the event of diode breakdown.

Referring to Figs. 5(a) and (b), which show another embodiment of the invention, a P⁺ type region 4 whose impurity concentration is about 10^{19} cm⁻³ is formed in the N⁺ type region 2 and substrate 1 near the P⁺ type region 3 shown in Figure 1. This P⁺ type 4 is used for connection to a grounding electrode 7. It is desirable that the distance between the P⁺ type regions 3 and 4 is determined so as not to cause punch-through phenomenon; practically, this distance is about 10 μ.

In the above arrangement, the circuit can be grounded with very low resistance via a metal lead 17 having a high conductivity. Therefore, the resistance component observed at the breakdown point can be markedly reduced. In the first embodiment described above, the breakdown current at a high voltage flows to the ground through the substrate whose impurity concentration is comparatively low. Whereas, in the second embodiment, the breakdown current can be grounded through a metal lead whereby it is possible to reduce the resistance component produced at the breakdown point.

The P⁺ type region 4 is in ohmic contact with the electrode 7. Instead, the conductivity type of the P⁺ type region 4 may be N⁺ type with high impurity concentration and such N⁺ type region 4 is used to secure an ohmic contact of the connection of the electrode 7 to the N⁺ type region 2. The electrode 7 may be directly brought into ohmic contact with the N⁺ type region 2, with region 4 omitted, where the impurity concentration in the N⁺ type region 2 is so high that a good ohmic contact may be formed between the region 2 and the electrode 7.

In the foregoing first and second embodiments, the N⁺ type region 2 is located adjacent to the terminal 6 of P⁺ type region 3, which terminal is used for connection of the gate electrode of an insulate-gate field effect transistor. Instead, the N⁺ type region 2 may be formed all over the surface of the substrate 1 except the gate region of the insulated-gate field effect transistor 100 and the P⁺ type regions. In this embodiment, the edge effect and the parasitic MOS effect observed due to channels formed in the part other than the gate region 18 (in Fig. 5(b)) of the insulated-gate field effect transistor

100 can be prevented. This is because the N type part between the P type regions excepting the N type gate region 18 (in Fig. 5(b)) of the field effect transistor 100, is made a high impurity concentration region and the voltage necessary to invert the conductivity type between said regions is high. As is apparent from the foregoing the present invention finds application mainly to MOS integrated circuit devices.

WHAT WE CLAIM IS:—

1. An insulated gate field effect transistor with means for protecting the transistor against the application of a high input voltage to the gate thereof, comprising a semiconductor substrate of a first conductivity type,

an insulated gate field effect transistor formed in said substrate and having source and drain regions and a gate electrode, said gate electrode being formed on an insulator film which is disposed on the substrate between said source and drain regions,

a first region formed on said substrate at a location spaced from said transistor and being of a conductivity type opposite to said first conductivity type, the first region having an input terminal at one end thereof and an output terminal at the other end thereof and forming a resistor between the input and output terminals, and

a second region formed on said substrate; said second region being in contact with said first region, being of the first conductivity type and having a high concentration of impurities, thereby to form with said first region a diode having a low breakdown voltage,

wherein the output terminal of said first region is connected to said gate electrode, and the gate insulator film of said transistor is protected against breakdown by a high

input voltage by said resistor and said diode.

2. A field effect transistor as claimed in claim 1, wherein said second region is in contact with said first region at the said one end of said first region.

3. A field effect transistor as claimed in claim 2, further comprising a third region of the conductivity type opposite to said first conductivity type, said third region having a high impurity concentration, being in contact with said second region, and being grounded by way of a wiring layer formed on said substrate.

4. A field effect transistor as claimed in claim 2, further comprising a fourth region of said first conductivity type, said fourth region having a high impurity concentration, being in contact with said second region, and being grounded by way of a wiring layer formed on said substrate.

5. A field effect transistor as claimed in claim 1, wherein said second region is grounded by way of a wiring layer formed on said substrate.

6. A field effect transistor as claimed in claim 1, wherein said second region is formed on the whole surface of said substrate except for said source and drain regions, said region between said source and drain regions, and the other region or regions of the conductivity type opposite to said first conductivity type.

7. An insulated gate field effect transistor constructed, arranged and adapted to operate substantially as hereinbefore described with reference to, and as illustrated in, Figures 2(a), 2(b), 3 and 4 or Figures 5(a) and 5(b) of the accompanying drawings.

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100 can be prevented. This is because the N type part between the P type regions excepting the N type gate region 18 (in Fig. 5(b)) of the field effect transistor 100, is made a high impurity concentration region and the voltage necessary to invert the conductivity type between said regions is high. As is apparent from the foregoing the present invention finds application mainly to MOS integrated circuit devices.

WHAT WE CLAIM IS:—

1. An insulated gate field effect transistor with means for protecting the transistor against the application of a high input voltage to the gate thereof, comprising a semiconductor substrate of a first conductivity type,
- an insulated gate field effect transistor formed in said substrate and having source and drain regions and a gate electrode, said gate electrode being formed on an insulator film which is disposed on the substrate between said source and drain regions,
- a first region formed on said substrate at a location spaced from said transistor and being of a conductivity type opposite to said first conductivity type, the first region having an input terminal at one end thereof and an output terminal at the other end thereof and forming a resistor between the input and output terminals, and
- a second region formed on said substrate; said second region being in contact with said first region, being of the first conductivity type and having a high concentration of impurities, thereby to form with said first region a diode having a low breakdown voltage,
- wherein the output terminal of said first region is connected to said gate electrode, and the gate insulator film of said transistor is protected against breakdown by a high

input voltage by said resistor and said diode.

2. A field effect transistor as claimed in claim 1, wherein said second region is in contact with said first region at the said one end of said first region.

3. A field effect transistor as claimed in claim 2, further comprising a third region of the conductivity type opposite to said first conductivity type, said third region having a high impurity concentration, being in contact with said second region, and being grounded by way of a wiring layer formed on said substrate.

4. A field effect transistor as claimed in claim 2, further comprising a fourth region of said first conductivity type, said fourth region having a high impurity concentration, being in contact with said second region, and being grounded by way of a wiring layer formed on said substrate.

5. A field effect transistor as claimed in claim 1, wherein said second region is grounded by way of a wiring layer formed on said substrate.

6. A field effect transistor as claimed in claim 1, wherein said second region is formed on the whole surface of said substrate except for said source and drain regions, said region between said source and drain regions, and the other region or regions of the conductivity type opposite to said first conductivity type.

7. An insulated gate field effect transistor constructed, arranged and adapted to operate substantially as hereinbefore described with reference to, and as illustrated in, Figures 2(a), 2(b), 3 and 4 or Figures 5(a) and 5(b) of the accompanying drawings.

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