

SINGLE CHAMBER FLOWABLE FILM FORMATION AND TREATMENTS

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims the benefit and priority of U.S. Patent Application No.

5 17/014,224, filed September 8, 2020, entitled “SINGLE CHAMBER FLOWABLE FILM FORMATION AND TREATMENTS”, which is hereby incorporated by reference in its entirety.

[0002] The present technology is related to the following applications, all concurrently filed 8 September 2020, and titled: “SEMICONDUCTOR PROCESSING CHAMBERS FOR

10 DEPOSITION AND ETCH” (Attorney docket number: 44018254US01 (1192137)), and “SEMICONDUCTOR PROCESSING CHAMBERS FOR DEPOSITION AND ETCH” (Attorney docket number: 44018155US01 (1190407)). Each of these applications is hereby incorporated by reference in their entirety for all purposes.

TECHNICAL FIELD

15 **[0003]** The present technology relates to semiconductor processing. More specifically, the present technology relates to systems and methods for depositing and treating materials including flowable films.

BACKGROUND

20 **[0004]** Integrated circuits are made possible by processes which produce intricately patterned material layers on substrate surfaces. Producing patterned material on a substrate requires controlled methods of formation and removal of exposed material. As device sizes continue to shrink, material formation may affect subsequent operations. For example, in gap filling
25 operations a material may be formed or deposited to fill a trench or other feature formed on a semiconductor substrate. As features may be characterized by higher aspect ratios and reduced critical dimensions, these filling operations may be challenged. For example, as the deposition may occur at the top and along sidewalls of the feature, continued deposition may pinch off the

feature including between sidewalls within the feature, and may produce voids within the feature. This can impact device performance and subsequent processing operations.

[0005] Thus, there is a need for improved systems and methods that can be used to produce high quality devices and structures. These and other needs are addressed by the present
5 technology.

SUMMARY

[0006] Exemplary processing methods may include forming a plasma of a silicon-containing precursor. The methods may include depositing a flowable film on a semiconductor substrate
10 with plasma effluents of the silicon-containing precursor. The semiconductor substrate may be housed in a processing region of a semiconductor processing chamber. The semiconductor substrate may define a feature within the semiconductor substrate. The processing region may at least partially be defined between a faceplate and a substrate support on which the semiconductor substrate is seated. The methods may include forming a treatment plasma within the processing
15 region of the semiconductor processing chamber. The treatment plasma may be formed at a first power level from a first power source. A second power may be applied to the substrate support from a second power source at a second power level. The methods may include densifying the flowable film within the feature defined within the semiconductor substrate with plasma effluents of the treatment plasma.

[0007] In some embodiments, the semiconductor processing chamber may be part of a semiconductor processing system. The system may include a chamber body. The system may include a pedestal configured to support a semiconductor substrate. The system may include a faceplate. The chamber body, the pedestal, and the faceplate may define the processing region. The system may include a high-frequency plasma source coupled with the faceplate. The high-
25 frequency plasma source may be the first power source. The system may include a low-frequency plasma source coupled with the pedestal. The low-frequency plasma source may be the second power source. The system may include a first L-C filter coupled with the pedestal and configured to virtually ground the high-frequency plasma source through the pedestal. The system may include a second L-C filter coupled with the faceplate and configured to virtually
30 ground the low-frequency plasma source to the chamber body.

[0008] The second power source may be operated in a pulsing mode at a pulsing frequency of less than or about 1 kHz. The first power source may be operated in a continuous wave mode during the treatment plasma while the second power source is operated in the pulsing mode. The second power source may be operated at a duty cycle of less than or about 50%. The first power source may be operated to produce a power spike within a first period of time during the depositing. Subsequent the first period of time, the first power source may be operated for a second period of time during the depositing. The first period of time may be less than or about one second, and the second period of time may be greater than or about one second. The first power source may be operated at a pulsing frequency of less than or about 200 kHz at a duty cycle of less than or about 20% to produce an effective plasma power of less than or about 10 W. The method may be repeated in a second cycle. A temperature of the semiconductor substrate may be maintained at a temperature of less than or about 0 °C during the method.

[0009] Some embodiments of the present technology may encompass semiconductor processing systems. The systems may include a chamber body. The systems may include a pedestal configured to support a semiconductor substrate. The systems may include a faceplate. The chamber body, the pedestal, and the faceplate may define a processing region. The systems may include a high-frequency plasma source coupled with the faceplate. The systems may include a low-frequency plasma source coupled with the pedestal.

[0010] In some embodiments, the pedestal may include an electrostatic chuck. The semiconductor processing system may include a DC power supply coupled with the pedestal. The low-frequency plasma source may be configured to operate at less than or about 2 MHz. The high-frequency plasma source may be configured to operate at greater than or about 13.56 MHz at a pulsing frequency of less than or about 200 kHz. The high-frequency plasma source may be configured to operate at a pulsing frequency of less than or about 20 kHz at a duty cycle of less than or about 20%. The high-frequency plasma source may be configured to generate a plasma at an effective power of less than or about 5 W. The systems may include a first L-C filter coupled with the pedestal and configured to virtually ground the high-frequency plasma source through the pedestal. The systems may include a second L-C filter coupled with the faceplate and configured to virtually ground the low-frequency plasma source to the chamber body.

[0011] Such technology may provide numerous benefits over conventional systems and techniques. For example, by performing a curing or treatment operation within the deposition chamber, throughput may be increased while sidewall coverage can be limited or controlled, which may limit void formation in small features. Additionally, by performing deposition according to embodiments of the present technology, repeatable plasma generation during deposition operations may be produced. These and other embodiments, along with many of their advantages and features, are described in more detail in conjunction with the below description and attached figures.

10

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] A further understanding of the nature and advantages of the disclosed technology may be realized by reference to the remaining portions of the specification and the drawings.

[0013] FIG. 1 shows a schematic cross-sectional view of an exemplary processing chamber according to some embodiments of the present technology.

15 [0014] FIG. 2 shows a schematic partial cross-sectional view of a chamber according to some embodiments of the present technology.

[0015] FIG. 3 shows exemplary operations in a processing method according to some embodiments of the present technology.

20 [0016] Several of the figures are included as schematics. It is to be understood that the figures are for illustrative purposes, and are not to be considered of scale unless specifically stated to be of scale. Additionally, as schematics, the figures are provided to aid comprehension and may not include all aspects or information compared to realistic representations, and may include exaggerated material for illustrative purposes.

25 [0017] In the appended figures, similar components and/or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a letter that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the letter.

DETAILED DESCRIPTION

[0018] Amorphous silicon may be used in semiconductor device manufacturing for a number of structures and processes, including as a sacrificial material, for example as a dummy gate material, or as a trench fill material. In gap filling operations, some processing may utilize flowable films formed under process conditions to limit conformality of deposition, which may allow the deposited material to better fill features on the substrate. Flowable silicon material may be characterized by relatively high amounts of hydrogen, and may be less dense than other formed films. Consequently, subsequent treatment operations may be performed to cure the produced films. Conventional technology may utilize a UV curing process to remove hydrogen and process the film. However, UV curing may result in significant film shrinkage, which may cause stress on features as well as produce voids within the structure. Additionally, the treatment is formed in a separate chamber from the deposition chamber, which will reduce throughput by increase processing time.

[0019] As feature sizes continue to shrink, flowable films may be challenged for narrow features, which may be further characterized by higher aspect ratios. For example, pinching of the feature may more readily occur due to deposition on sidewalls of the feature, which in small feature sizes may further restrict flow further into the feature, and may produce voids. Some conventional flowable film formation may be performed by producing radicals in a remote capacitively-coupled plasma region or in a remote plasma source unit coupled with the chamber. However, for cyclic formation in high aspect ratio features, this process may provide unreliable deposition. For example, as radicals pass through chamber components, such as a faceplate, recombination may challenge consistent provision of radical effluents. Additionally, remote plasma sources may be incapable of limiting an amount of deposition within small-pitch features. This may over-deposit within the feature, which may then limit or prevent complete penetration of treatment effluents. This may cause damage during later processing, which may lead to scrapped substrates.

[0020] The present technology may overcome these limitations by decoupling high-frequency and low-frequency power sources and utilizing a trigger sequence allowing a low-power, repeatable plasma generation to be performed for short periods of time. This may limit

deposition during trench fill to a tightly controlled amount, as well as assuring complete treatment during a subsequent treatment operation. After describing general aspects of a chamber according to some embodiments of the present technology in which plasma processing operations discussed below may be performed, specific chamber configurations and methodology may be discussed. It is to be understood that the present technology is not intended to be limited to the specific films, chambers, or processing discussed, as the techniques described may be used to improve a number of film formation processes for any number of materials, and may be applicable to a variety of processing chambers and operations.

[0021] FIG. 1 shows a cross-sectional view of an exemplary processing chamber 100 according to some embodiments of the present technology. The figure may illustrate an overview of a system incorporating one or more aspects of the present technology, and/or which may perform one or more deposition or other processing operations according to embodiments of the present technology. Additional details of chamber 100 or methods performed may be described further below. Chamber 100 may be utilized to form film layers according to some embodiments of the present technology, although it is to be understood that the methods may similarly be performed in any chamber within which film formation may occur. The processing chamber 100 may include a chamber body 102, a substrate support 104 disposed inside the chamber body 102, and a lid assembly 106 coupled with the chamber body 102 and enclosing the substrate support 104 in a processing volume 120. A substrate 103 may be provided to the processing volume 120 through an opening 126, which may be conventionally sealed for processing using a slit valve or door. The substrate 103 may be seated on a surface 105 of the substrate support during processing. The substrate support 104 may be rotatable, as indicated by the arrow 145, along an axis 147, where a shaft 144 of the substrate support 104 may be located. Alternatively, the substrate support 104 may be lifted up to rotate as necessary during a deposition process.

[0022] A plasma profile modulator 111 may be disposed in the processing chamber 100 to control plasma distribution across the substrate 103 disposed on the substrate support 104. The plasma profile modulator 111 may include a first electrode 108 that may be disposed adjacent to the chamber body 102, and may separate the chamber body 102 from other components of the lid assembly 106. The first electrode 108 may be part of the lid assembly 106, or may be a separate

sidewall electrode. The first electrode 108 may be an annular or ring-like member, and may be a ring electrode. The first electrode 108 may be a continuous loop around a circumference of the processing chamber 100 surrounding the processing volume 120, or may be discontinuous at selected locations if desired. The first electrode 108 may also be a perforated electrode, such as
5 a perforated ring or a mesh electrode, or may be a plate electrode, such as, for example, a secondary gas distributor.

[0023] One or more isolators 110a, 110b, which may be a dielectric material such as a ceramic or metal oxide, for example aluminum oxide and/or aluminum nitride, may contact the first electrode 108 and separate the first electrode 108 electrically and thermally from a gas distributor
10 112 and from the chamber body 102. The gas distributor 112 may define apertures 118 for distributing process precursors into the processing volume 120. The gas distributor 112 may be coupled with a first source of electric power 142, such as an RF generator, RF power source, DC power source, pulsed DC power source, pulsed RF power source, or any other power source that may be coupled with the processing chamber. In some embodiments, the first source of electric
15 power 142 may be an RF power source.

[0024] The gas distributor 112 may be a conductive gas distributor or a non-conductive gas distributor. The gas distributor 112 may also be formed of conductive and non-conductive components. For example, a body of the gas distributor 112 may be conductive while a face plate of the gas distributor 112 may be non-conductive. The gas distributor 112 may be
20 powered, such as by the first source of electric power 142 as shown in FIG. 1, or the gas distributor 112 may be coupled with ground in some embodiments.

[0025] The first electrode 108 may be coupled with a first tuning circuit 128 that may control a ground pathway of the processing chamber 100. The first tuning circuit 128 may include a first electronic sensor 130 and a first electronic controller 134. The first electronic controller 134
25 may be or include a variable capacitor or other circuit elements. The first tuning circuit 128 may be or include one or more inductors 132. The first tuning circuit 128 may be any circuit that enables variable or controllable impedance under the plasma conditions present in the processing volume 120 during processing. In some embodiments as illustrated, the first tuning circuit 128 may include a first circuit leg and a second circuit leg coupled in parallel between ground and the
30 first electronic sensor 130. The first circuit leg may include a first inductor 132A. The second

circuit leg may include a second inductor 132B coupled in series with the first electronic controller 134. The second inductor 132B may be disposed between the first electronic controller 134 and a node connecting both the first and second circuit legs to the first electronic sensor 130. The first electronic sensor 130 may be a voltage or current sensor and may be
5 coupled with the first electronic controller 134, which may afford a degree of closed-loop control of plasma conditions inside the processing volume 120.

[0026] A second electrode 122 may be coupled with the substrate support 104. The second electrode 122 may be embedded within the substrate support 104 or coupled with a surface of the substrate support 104. The second electrode 122 may be a plate, a perforated plate, a mesh, a
10 wire screen, or any other distributed arrangement of conductive elements. The second electrode 122 may be a tuning electrode, and may be coupled with a second tuning circuit 136 by a conduit 146, for example a cable having a selected resistance, such as 50 ohms, for example, disposed in the shaft 144 of the substrate support 104. The second tuning circuit 136 may have a second electronic sensor 138 and a second electronic controller 140, which may be a second variable
15 capacitor. The second electronic sensor 138 may be a voltage or current sensor, and may be coupled with the second electronic controller 140 to provide further control over plasma conditions in the processing volume 120.

[0027] A third electrode 124, which may be a bias electrode and/or an electrostatic chucking electrode, may be coupled with the substrate support 104. The third electrode may be coupled
20 with a second source of electric power 150 through a filter 148, which may be an impedance matching circuit. The second source of electric power 150 may be DC power, pulsed DC power, RF bias power, a pulsed RF source or bias power, or a combination of these or other power sources. In some embodiments, the second source of electric power 150 may be an RF bias power.

[0028] The lid assembly 106 and substrate support 104 of FIG. 1 may be used with any
25 processing chamber for plasma or thermal processing. In operation, the processing chamber 100 may afford real-time control of plasma conditions in the processing volume 120. The substrate 103 may be disposed on the substrate support 104, and process gases may be flowed through the lid assembly 106 using an inlet 114 according to any desired flow plan. Gases may exit the
30 processing chamber 100 through an outlet 152. Electric power may be coupled with the gas

distributor 112 to establish a plasma in the processing volume 120. The substrate may be subjected to an electrical bias using the third electrode 124 in some embodiments.

[0029] Upon energizing a plasma in the processing volume 120, a potential difference may be established between the plasma and the first electrode 108. A potential difference may also be established between the plasma and the second electrode 122. The electronic controllers 134, 140 may then be used to adjust the flow properties of the ground paths represented by the two tuning circuits 128 and 136. A set point may be delivered to the first tuning circuit 128 and the second tuning circuit 136 to provide independent control of deposition rate and of plasma density uniformity from center to edge. In embodiments where the electronic controllers may both be variable capacitors, the electronic sensors may adjust the variable capacitors to maximize deposition rate and minimize thickness non-uniformity independently.

[0030] Each of the tuning circuits 128, 136 may have a variable impedance that may be adjusted using the respective electronic controllers 134, 140. Where the electronic controllers 134, 140 are variable capacitors, the capacitance range of each of the variable capacitors, and the inductances of the first inductor 132A and the second inductor 132B, may be chosen to provide an impedance range. This range may depend on the frequency and voltage characteristics of the plasma, which may have a minimum in the capacitance range of each variable capacitor. Hence, when the capacitance of the first electronic controller 134 is at a minimum or maximum, impedance of the first tuning circuit 128 may be high, resulting in a plasma shape that has a minimum aerial or lateral coverage over the substrate support. When the capacitance of the first electronic controller 134 approaches a value that minimizes the impedance of the first tuning circuit 128, the aerial coverage of the plasma may grow to a maximum, effectively covering the entire working area of the substrate support 104. As the capacitance of the first electronic controller 134 deviates from the minimum impedance setting, the plasma shape may shrink from the chamber walls and aerial coverage of the substrate support may decline. The second electronic controller 140 may have a similar effect, increasing and decreasing aerial coverage of the plasma over the substrate support as the capacitance of the second electronic controller 140 may be changed.

[0031] The electronic sensors 130, 138 may be used to tune the respective circuits 128, 136 in a closed loop. A set point for current or voltage, depending on the type of sensor used, may be

installed in each sensor, and the sensor may be provided with control software that determines an adjustment to each respective electronic controller 134, 140 to minimize deviation from the set point. Consequently, a plasma shape may be selected and dynamically controlled during processing. It is to be understood that, while the foregoing discussion is based on electronic
5 controllers 134, 140, which may be variable capacitors, any electronic component with adjustable characteristic may be used to provide tuning circuits 128 and 136 with adjustable impedance.

[0032] FIG. 2 shows a schematic partial cross-sectional view of a processing chamber 200 according to some embodiments of the present technology. Chamber 200 may include any
10 feature, component, or characteristic of processing chamber 100 described above, and may illustrate additional features of the chamber, including specific power source coupling with the chamber. For example, chamber 200 may include a chamber body 205. The chamber may include a substrate support 210, which may be configured to support a substrate during semiconductor processing. The chamber may include a faceplate 215, which with the pedestal
15 and chamber body may define a processing region above a substrate being processed.

[0033] Some conventional processing systems may generate a plasma within the processing region by applying power to the faceplate while grounding the pedestal, or applying source power to the pedestal and grounding the faceplate. In some systems an additional bias power may be coupled with the pedestal to increase directionality of plasma effluents. It is to be
20 understood that a separate DC power supply for electrostatic chucking may be coupled with the pedestal as previously described with processing chamber 100, which may also be operated to further bias a produced plasma within the processing chamber in addition to chucking the substrate. The present technology may differ from conventional configurations by coupling two separate plasma power sources with the showerhead and pedestal as illustrated. For example, a
25 first plasma power source 220 may be coupled with the showerhead, and a second plasma power source 230 may be coupled with the pedestal. In some embodiments the first plasma power source 220 may be a high-frequency plasma power source, and the second plasma power source 230 may be a low-frequency plasma power source. In some embodiments, low-frequency plasma power source 230 may be separate from a DC power source, which may be used for
30 electrostatic coupling a substrate to the pedestal.

[0034] The low-frequency plasma power source may operate at a first frequency that is less than or about 2 MHz, and may operate at a frequency that is less than or about 1.5 MHz, less than or about 1.0 MHz, less than or about 800 kHz, less than or about 600 kHz, less than or about 500 kHz, less than or about 400 kHz, less than or about 350 kHz, less than or about 300 kHz, less than or about 250 kHz, less than or about 200 kHz, or less. The high-frequency plasma power source may operate at a second frequency that is greater than or about 2 MHz, and may be greater than or about 10 MHz, greater than or about 13 MHz, such as 13.56 MHz, greater than or about 15 MHz, greater than or about 20 MHz, greater than or about 40 MHz, or higher.

[0035] Additional aspects of the plasma sources may be used to further tune the generated plasma within the processing region. For example, chambers according to embodiments of the present technology may be used to fill high-aspect ratio features, where a discreet amount of deposition may be produced to limit void formation within the feature being filled. Conventional chambers may be limited in a reduction of plasma power based on an inability to produce a repeatable low-power plasma for a limited period of time. The present technology may be used to produce material layers characterized by a thickness of less than or about 10 nm per cycle. To accomplish this limited deposition, either the deposition period may be limited, or the power used during deposition may be reduced. Conventional systems may not be capable of reducing plasma power below or about 100 W, which may increase the amount of deposition material, and reducing the formation period to accommodate this higher power may limit the ability to produce a repeatable plasma during a multiple cycle deposition.

[0036] The present technology overcomes these issues by producing a low-power deposition plasma, which may be characterized by an effective plasma power of less than or about 20 W, and may be characterized by an effective plasma power of less than or about 15 W, less than or about 10 W, less than or about 8 W, less than or about 6 W, less than or about 5 W, less than or about 4 W, less than or about 3 W, or less. To produce this lower power plasma during a deposition operation, the system may operate the high-frequency plasma power at a pulsing frequency of less than or about 200 kHz, and may operate the plasma power at a pulsing frequency of less than or about 150 kHz, less than or about 100 kHz, less than or about 80 kHz, less than or about 70 kHz, less than or about 60 kHz, less than or about 50 kHz, less than or about 40 kHz, less than or about 30 kHz, less than or about 20 kHz, less than or about 10 kHz, or

less. Additionally, and at any of the pulsing frequencies noted, the high-frequency plasma power source may be operated at a reduced duty cycle, which may be less than or about 50%, and may be less than or about 45%, less than or about 40%, less than or about 35%, less than or about 30%, less than or about 25%, less than or about 20%, less than or about 15%, less than or about 10%, less than or about 5%, or less.

[0037] In some embodiments, the reduced pulsing frequency and duty cycle, may challenge plasma generation in a consistent manner. The low-power plasma once generated may produce a low-rate deposition to limit deposition per cycle, however, ignition may be challenged. Accordingly, in some embodiments, the plasma power may operate with a trigger sequence to facilitate plasma generation during deposition. For example, as noted above, in some embodiments the deposition operation may be performed without the low-frequency plasma power source. However, in some embodiments during the deposition operation, the low-frequency plasma power source may be operated to facilitate ignition. Additionally, the low-frequency plasma power source may not be operated, and a power spike may be applied with the high-frequency plasma power source to facilitate ignition. The power spike may be applied directly with power management, or through a level-to-level operation of the high-frequency plasma power source.

[0038] The low-frequency plasma power source may also be operated to control plasma formation and ion directionality during processing. By delivering the low-frequency plasma power through the pedestal, the plasma sheath formed at this powered electrode may benefit directionality of ions into the feature being densified. The low-frequency plasma power source may be operated at any of the power levels or pulsing frequencies noted above, although in some embodiments the second power source 230 may be operated at a greater plasma power than the first power source 220 during a treatment operation. For example, during the treatment the plasma power delivered by the second power source may be greater than or about 50 W, and may be greater than or about 100 W, greater than or about 200 W, greater than or about 300 W, greater than or about 400 W, greater than or about 500 W, greater than or about 600 W, greater than or about 700 W, greater than or about 800 W, or more. By increasing the plasma power of the low-frequency power supply during the treatment plasma formation, a greater amount of

plasma effluents may be generated. Applying greater low-frequency power from the pedestal may increase a directionality of delivery perpendicular to a plane across the substrate.

[0039] Additional adjustments may be made to further increase etching of deposited material along sidewalls of the features by adjusting one or more characteristics of the plasma power or bias power being supplied. For example, in some embodiments both the plasma power source and bias power source may be operated in a continuous wave mode. Additionally, one or both of the power sources may be operated in a pulsed mode. In some embodiments, the high-frequency source power may be operated in a continuous wave mode or pulsed mode while the low-frequency power may be operated in a pulsed mode during the treatment. A pulsing frequency for the low-frequency plasma power source may be less than or about 1,000 Hz, and may be less than or about 900 Hz, less than or about 800 Hz, less than or about 700 Hz, less than or about 600 Hz, less than or about 500 Hz, less than or about 400 Hz, less than or about 300 Hz, less than or about 200 Hz, less than or about 100 Hz, or less. The duty cycle of the second power supply may be less than or about 50%, and the low-frequency plasma power may be operated at a duty cycle of less than or about 45%, less than or about 40%, less than or about 35%, less than or about 30%, less than or about 25%, less than or about 20%, less than or about 15%, less than or about 10%, less than or about 5%, or less. By operating the low-frequency power at a reduced duty cycle, such as an on-time duty of less than or about 50%, a greater amount of time per cycle may be performing a more isotropic etch within the feature based on operation of the high-frequency power supply, which may better remove material from the sidewalls during a densification operation.

[0040] The first plasma power source 220 may be coupled with ground virtually through the pedestal. For example, as illustrated, a first L-C filter 225 may be coupled with the pedestal and may virtually ground the high-frequency plasma source through the pedestal. Similarly, the second plasma power source 230 may be coupled with ground through the chamber. For example, a second L-C filter may be coupled with the faceplate, which may virtually ground the low-frequency plasma source, such as to the chamber body or an external ground. By separating the high-frequency power supply and the low-frequency power supply, improved plasma generation and operation may be provided.

[0041] Processing chamber 100 and/or processing chamber 200 may be utilized in some embodiments of the present technology for processing methods that may include formation, etching, or curing of materials for semiconductor structures. It is to be understood that the chamber described is not to be considered limiting, and any chamber that may be configured to perform operations as described may be similarly used. **FIG. 3** shows exemplary operations in a processing method 300 according to some embodiments of the present technology. The method may be performed in a variety of processing chambers and on one or more mainframes or tools, including processing chamber 100 or processing chamber 200 described above. Method 300 may include a number of optional operations, which may or may not be specifically associated with some embodiments of methods according to the present technology. For example, many of the operations are described in order to provide a broader scope of the structural formation, but are not critical to the technology, or may be performed by alternative methodology as would be readily appreciated.

[0042] Method 300 may include additional operations prior to initiation of the listed operations. For example, additional processing operations may include forming structures on a semiconductor substrate, which may include both forming and removing material. For example, transistor structures, memory structures, or any other structures may be formed. Prior processing operations may be performed in the chamber in which method 300 may be performed, or processing may be performed in one or more other processing chambers prior to delivering the substrate into the semiconductor processing chamber or chambers in which method 300 may be performed. Regardless, method 300 may optionally include delivering a semiconductor substrate to a processing region of a semiconductor processing chamber, such as processing chamber 200 described above, or other chambers that may include components as described above. The substrate may be deposited on a substrate support, which may be a pedestal such as substrate support 210, and which may reside in a processing region of the chamber, such as processing volume 120 described above.

[0043] A substrate to be processed may be or include any number of materials used in semiconductor processing. The substrate material may be or include silicon, germanium, dielectric materials including silicon oxide or silicon nitride, metal materials, or any number of combinations of these materials, which may be the substrate or materials formed on the structure.

Features may be characterized by any shape or configuration according to the present technology. In some embodiments, the features may be or include a trench structure or aperture formed within the substrate. Although the features may be characterized by any shapes or sizes, in some embodiments the features may be characterized by higher aspect ratios, or a ratio of a depth of the feature to a width across the feature. For example, in some embodiments features may be characterized by aspect ratios greater than or about 5:1, and may be characterized by aspect ratios greater than or about 10:1, greater than or about 15:1, greater than or about 20:1, greater than or about 25:1, greater than or about 30:1, greater than or about 40:1, greater than or about 50:1, or greater. Additionally, the features may be characterized by narrow widths or diameters across the feature including between two sidewalls, such as a dimension less than or about 20 nm, and may be characterized by a width across the feature of less than or about 15 nm, less than or about 12 nm, less than or about 10 nm, less than or about 9 nm, less than or about 8 nm, less than or about 7 nm, less than or about 6 nm, less than or about 5 nm, or less.

[0044] In some embodiments, method 300 may include optional treatment operations, such as a pretreatment, that may be performed to prepare a surface of the substrate for deposition. Once prepared, method 300 may include delivering one or more precursors to a processing region of the semiconductor processing chamber housing the structure. The precursors may include one or more silicon-containing precursors, as well as one or more diluents or carrier gases such as an inert gas or other gas delivered with the silicon-containing precursor. Although the present method will be explained in relation to producing a flowable silicon film, it is to be understood the method and/or chambers described may be used to produce any number of materials according to embodiments of the present technology. A plasma may be formed of the deposition precursors including the silicon-containing precursor at operation 305. The plasma may be formed within the processing region, which may allow deposition materials to deposit on the substrate. For example, in some embodiments a capacitively-coupled plasma may be formed within the processing region by applying plasma power to the faceplate as previously described. For example, a high-frequency power supply as discussed above may be operated at a reduced effective plasma power to deposit materials within the features on the substrate.

[0045] A silicon-containing material may be deposited on the substrate at operation 310 from plasma effluents of the silicon-containing precursor. The material may be a flowable silicon-

containing material in some embodiments, which may be or include amorphous silicon. The deposited materials may at least partially flow into the features on the substrate to provide a bottom-up type of gap fill. The deposited material may flow into the bottom of the feature, although an amount of material may remain on the sidewalls of the substrate as illustrated.

- 5 Although the amount deposited may be relatively small, the remaining material on the sidewalls may limit subsequent flow.

[0046] The power applied during deposition may be a lower power plasma, which may limit dissociation, and which may maintain an amount of hydrogen incorporation in the deposited materials. This incorporated hydrogen may contribute to the flowability of the materials deposited. Accordingly, in some embodiments a plasma power source may deliver a plasma power to the faceplate of less than or about 100 W, and may deliver a power of less than or about 90 W, less than or about 80 W, less than or about 70 W, less than or about 60 W, less than or about 50 W, or less. This power may be further attenuated by operating the high-frequency power supply at a pulsing frequency and duty cycle as previously explained, which may produce an effective power below or about 10 W, and may produce an effective power below or about 5 W, as discussed above.

[0047] Subsequent an amount of deposition, in some embodiments of the present technology a treatment or curing process may be formed that is configured to densify the formed material, and may beneficially clean or etch back material on the sidewalls of the feature. This process may be performed in the same chamber as the deposition, and may be performed in a cyclic process to fill the feature. In some embodiments the silicon-containing precursor flow may be halted and the processing region may be purged. Subsequent a purge, a treatment precursor may be flowed into the processing region of the processing chamber. The treatment precursor may be or include hydrogen, helium, argon, or another inert material, which may not be chemically reactive with the film. A treatment plasma may be formed at operation 315, which may also be a capacitively-coupled plasma formed within the processing region. While the deposition plasma formed may be formed by applying a high-frequency plasma power to the faceplate or showerhead, and which in some embodiments may not include another power source being engaged. The treatment may utilize both the high-frequency power supply as well as a low-frequency power supply coupled with the substrate support as previously discussed. The high-frequency power

supply may be operated at a first power level and the low-frequency power supply may be operated at a second power level during the treatment, and the two power levels may be similar or different in embodiments of the present technology.

[0048] While the high-frequency power supply may be operated at a pulsed and low-effective power during the deposition plasma, the high-frequency power supply may be operated in a continuous wave configuration during the treatment, which may be at any of the plasma powers previously described. The low-frequency power supply may be operated in a pulsing mode during the treatment, which may be at any of the pulsing frequencies and/or duty cycles as previously described.

[0049] During the deposition operation, the low-frequency power supply may not be operated. As discussed above, to enable a repeatable plasma generation at low power, a trigger sequence may be utilized to ensure plasma generation during each deposition operation. The trigger sequence may include a first period of time and a second period of time, which together may create a deposition period of time. To limit deposition in some embodiments, the deposition period of time may be less than or about 30 seconds, and may be less than or about 20 seconds, less than or about 15 seconds, less than or about 10 seconds, less than or about 8 seconds, less than or about 6 seconds, less than or about 5 seconds, less than or about 4 seconds, or less. The first period of time may be less than the second period of time, and the first period of time may be used to ensure plasma generation occurs, while limiting an effect on the deposition process. Accordingly, in some embodiments the first period of time may be less than or about 2 seconds, and may be less than or about 1 second, less than or about 0.5 seconds, less than or about 0.4 seconds, less than or about 0.3 seconds, less than or about 0.2 seconds, less than or about 0.1 seconds, less than or about 0.09 seconds, less than or about 0.08 seconds, less than or about 0.07 seconds, less than or about 0.06 seconds, less than or about 0.05 seconds, or less.

[0050] In some embodiments a first power may be applied by the high-frequency power source during the first period of time, which may be higher than a second power applied by the high-frequency power source during the second period of time. For example, during the first period of time, the first power may be greater than or about 50 W, and may be greater than or about 80 W, greater than or about 100 W, greater than or about 120 W, greater than or about 140 W, greater than or about 160 W, greater than or about 180 W, greater than or about 200 W, or higher. The

high-frequency power source may then apply power during the second period of time at any of the effective powers discussed above during the remainder of the deposition time. Additionally, the high-frequency power source may be operated consistently during the deposition time, but during the first period of time the low-frequency power source may be applied at any power level discussed above to ensure ignition. In another example, the high-frequency power supply may be operated in a multi-level pulsing configuration during the first period of time before switching the desired effective power during the second period of time. The multi-level pulsing may include a number of pulses, which may each be less than 0.1 seconds, for example, such as less than or about 50 microseconds, less than or about 40 microseconds, less than or about 30 microseconds, less than or about 20 microseconds, or less, and which all occur during the first period of time. The pulses may include a higher initial pulse for a first fraction of the pulse, followed by a lower second pulse for a second fraction of the pulse. The two portions of the pulse may occur at any power levels previously described.

[0051] During the treatment operation, the plasma effluents may optionally at least partially etch the flowable film at operation 320, and may remove the flowable film from the sidewalls of the trench. Simultaneously, or additionally, plasma effluents delivered more directionally may penetrate the remaining film formed at the bottom of the feature, and may reduce hydrogen incorporation to densify the film at operation 325.

[0052] Although the deposition may be formed to several nanometers or more, by performing an etch process as previously described, the thickness of densified material may be controlled to be at a thickness of less than or about 100 Å, and may be less than or about 90 Å, less than or about 80 Å, less than or about 70 Å, less than or about 60 Å, less than or about 50 Å, less than or about 40 Å, less than or about 30 Å, less than or about 20 Å, less than or about 10 Å, or less. By controlling the thickness of the deposited material, conversion through the entire thickness may be performed more readily, and penetration issues common in conventional processes may be resolved. The process may then be fully repeated for any number of cycles to continue to produce the densified material up through the feature.

[0053] Any number of precursors may be used with the present technology with regard to the deposition precursors used during any of the formation operations. Silicon-containing precursors that may be used during may include, but are not limited to, silane (SiH_4), disilane (Si_2H_6), or

other organosilanes including cyclohexasilanes, silicon tetrafluoride (SiF₄), silicon tetrachloride (SiCl₄), dichlorosilane (SiH₂Cl₂), tetraethyl orthosilicate (TEOS), as well as any other silicon-containing precursors that may be used in silicon-containing film formation. The silicon-containing material may be nitrogen-free, oxygen-free, and/or carbon-free in some embodiments.

- 5 In any of the operations one or more additional precursors may be included, such as inert precursors, which may include Ar, diatomic hydrogen, He, or other materials such as nitrogen, ammonia, or other precursors.

[0054] Temperature and pressure may also impact operations of the present technology. For example, in some embodiments to facilitate film flow, the process may be performed at a
10 temperature below or about 20 °C, and may be performed at a temperature less than or about 10 °C, less than or about 0 °C, less than or about -10 °C, less than or about -20 °C, less than or about -30 °C, or lower. The temperature may be maintained in any of these ranges throughout the method, including during the treatment and densifying. Pressure within the chamber may be kept relatively low for any of the processes as well, such as at a chamber pressure of less than or
15 about 10 Torr, and pressure may be maintained at less than or about 8 Torr, less than or about 6 Torr, less than or about 5 Torr, less than or about 4 Torr, less than or about 3 Torr, less than or about 2 Torr, less than or about 1 Torr, or less. Additionally, the pressure may be maintained at different levels during the deposition and the treatment in some embodiments. For example, the pressure may be maintained greater than or about 1 Torr during the deposition, such as greater
20 than or about 2 Torr, greater than or about 3 Torr, or higher, and the pressure may be maintained less than or about 1 Torr during the treatment, such as less than or about 0.8 Torr, less than or about 0.5 Torr, less than or about 0.1 Torr, or less. By performing processes according to some embodiments of the present technology, improved fill of narrow features utilizing silicon-containing or other flowable materials may be produced.

- 25 [0055] In the preceding description, for the purposes of explanation, numerous details have been set forth in order to provide an understanding of various embodiments of the present technology. It will be apparent to one skilled in the art, however, that certain embodiments may be practiced without some of these details, or with additional details.

[0056] Having disclosed several embodiments, it will be recognized by those of skill in the art
30 that various modifications, alternative constructions, and equivalents may be used without

departing from the spirit of the embodiments. Additionally, a number of well-known processes and elements have not been described in order to avoid unnecessarily obscuring the present technology. Accordingly, the above description should not be taken as limiting the scope of the technology. Additionally, methods or processes may be described as sequential or in steps, but it is to be understood that the operations may be performed concurrently, or in different orders than listed.

[0057] Where a range of values is provided, it is understood that each intervening value, to the smallest fraction of the unit of the lower limit, unless the context clearly dictates otherwise, between the upper and lower limits of that range is also specifically disclosed. Any narrower range between any stated values or unstated intervening values in a stated range and any other stated or intervening value in that stated range is encompassed. The upper and lower limits of those smaller ranges may independently be included or excluded in the range, and each range where either, neither, or both limits are included in the smaller ranges is also encompassed within the technology, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included.

[0058] As used herein and in the appended claims, the singular forms “a”, “an”, and “the” include plural references unless the context clearly dictates otherwise. Thus, for example, reference to “a precursor” includes a plurality of such precursors, and reference to “the layer” includes reference to one or more layers and equivalents thereof known to those skilled in the art, and so forth.

[0059] Also, the words “comprise(s)”, “comprising”, “contain(s)”, “containing”, “include(s)”, and “including”, when used in this specification and in the following claims, are intended to specify the presence of stated features, integers, components, or operations, but they do not preclude the presence or addition of one or more other features, integers, components, operations, acts, or groups.

CLAIMS:

1. A processing method comprising:
forming a plasma of a silicon-containing precursor;
depositing a flowable film on a semiconductor substrate with plasma effluents of
5 the silicon-containing precursor, wherein the semiconductor substrate is housed in a processing
region of a semiconductor processing chamber, wherein the semiconductor substrate defines a
feature within the semiconductor substrate, and wherein the processing region is at least partially
defined between a faceplate and a substrate support on which the semiconductor substrate is
seated;
10 forming a treatment plasma within the processing region of the semiconductor
processing chamber, wherein the treatment plasma is formed at a first power level from a first
power source, and wherein a second power level is applied to the substrate support from a
second power source; and
densifying the flowable film within the feature defined within the semiconductor
15 substrate with plasma effluents of the treatment plasma.
2. The processing method of claim 1, wherein the semiconductor processing
chamber is part of a semiconductor processing system comprising:
a chamber body;
a pedestal configured to support a semiconductor substrate;
20 a faceplate, wherein the chamber body, the pedestal, and the faceplate define the
processing region;
a high-frequency plasma source coupled with the faceplate, wherein the high-
frequency plasma source is the first power source; and
a low-frequency plasma source coupled with the pedestal, wherein the low-
25 frequency plasma source is the second power source.
3. The processing method of claim 2, further comprising:
a first L-C filter coupled with the pedestal and configured to virtually ground the
high-frequency plasma source through the pedestal, and

a second L-C filter coupled with the faceplate and configured to virtually ground the low-frequency plasma source to the chamber body.

4. The processing method of claim 1, wherein the second power source is operated in a pulsing mode at a pulsing frequency of less than or about 1 kHz.

5 5. The processing method of claim 4, wherein the first power source is operated in a continuous wave mode during the treatment plasma while the second power source is operated in the pulsing mode.

6. The processing method of claim 4, wherein the second power source is operated at a duty cycle of less than or about 50%.

10 7. The processing method of claim 1, wherein the first power source is operated to produce a power spike within a first period of time during the depositing.

8. The processing method of claim 7, wherein, subsequent the first period of time, the first power source is operated for a second period of time during the depositing.

15 9. The processing method of claim 8, wherein the first period of time is less than or about one second, and wherein the second period of time is greater than or about one second.

10. The processing method of claim 9, wherein the first power source is operated at a pulsing frequency of less than or about 200 kHz at a duty cycle of less than or about 20% to produce an effective plasma power of less than or about 10 W.

20 11. The processing method of claim 1, wherein the method is repeated in a second cycle.

12. The processing method of claim 1, wherein a temperature of the semiconductor substrate is maintained at a temperature of less than or about 0 °C during the method.

25 13. A semiconductor processing system comprising:

a chamber body;
a pedestal configured to support a semiconductor substrate;
a faceplate, wherein the chamber body, the pedestal, and the faceplate define a processing region;
5 a high-frequency plasma source coupled with the faceplate; and
a low-frequency plasma source coupled with the pedestal.

14. The semiconductor processing system of claim 13, wherein the pedestal comprises an electrostatic chuck, the semiconductor processing system further comprising:
a DC power supply coupled with the pedestal.

10 15. The semiconductor processing system of claim 13, wherein the low-frequency plasma source is configured to operate at less than or about 2 MHz.

16. The semiconductor processing system of claim 13, wherein the high-frequency plasma source is configured to operate at greater than or about 13.56 MHz at a pulsing frequency of less than or about 200 kHz.

15 17. The semiconductor processing system of claim 16, wherein the high-frequency plasma source is configured to operate at a pulsing frequency of less than or about 20 kHz at a duty cycle of less than or about 20%.

18. The semiconductor processing system of claim 17, wherein the high-frequency plasma source is configured to generate a plasma at an effective power of less than or
20 about 5 W.

19. The semiconductor processing system of claim 13, further comprising:
a first L-C filter coupled with the pedestal and configured to virtually ground the high-frequency plasma source through the pedestal.

20. The semiconductor processing system of claim 19, further comprising
25 a second L-C filter coupled with the faceplate and configured to virtually ground the low-frequency plasma source to the chamber body.