Abstract

Method For Fabricating a Planar Field Oxide Region

The present invention provides a method of manufacturing a planar field isolation region using a polysilicon layer as a polishing stop. The method begins by sequentially forming an insulating layer 12, a polysilicon layer 14 and a nitride layer 16 over a primary surface of a substrate 10. The polysilicon layer 14 and the nitride layer 16 are patterned to form a first opening exposing insulating layer 12. A field isolation region is grown to a first thickness within the first opening. The nitride layer is removed. The field isolation region is polished so that the top surface of the field isolation region is coplanar with the top surface of the polysilicon layer. Next the polysilicon layer is removed by either of two embodiments. First, the polysilicon is removed by a second (CMP) polishing step which uses a different slurry than the field oxide CMP. The second CMP step the exposed surface of the field isolation region is coplanar with an exposed surface of the polysilicon layer. Second, the polysilicon layer can be removed by a selective etch.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)