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SILICON-RICH OXIDE FOR COPPER DAMASCENE INTERCONNECT INCORPORATING LOW DIELECTRIC CONSTANT DIELECTRICS

The present invention relates generally to fabrication of semiconductor devices, and more specifically to etch stop layers used in fabrication processes of semiconductor devices.

BACKGROUND OF THE INVENTION

Currently, silicon nitride (SiN) or silicon oxynitride (SiON) liners are chosen as the etch stop layer and as hard masks for fluorine (F)-doped and carbon (C)-doped low-k dielectrics like FSG, CORAL™, BLACK DIAMOND™, SiLK™, etc. in copper (Cu) single/dual damascene interconnect processes. However, it has been reported that using either SiN (having a dielectric constant of about 7.0) or SiON (having a dielectric constant of about 5.5) causes masking footing and via poisoning issues due to the interaction of photoresist with amine species. Further, the high dielectric constant (k) from SiN or SiON compensates the effect of introducing low-k material into semiconductor manufacturing and results in a high effective dielectric constant of intermetal dielectric (IMD) layers.

U.S. Patent No. 6,207,556 B1 to Hsu describes an silicon-rich oxide (SRO) layer 204 and low-k layers.

U.S. Patent No. 6,174,797 B1 to Bao et al. describes an SRO barrier layer 16.

U.S. Patent No. 6,228,756 B1 to Lee describes a silicon-rich layer 114 for low-k layer 106.

U.S. Patent Nos. 6,166,427 to Huang et al., 6,133,143 to Lin et al. and 5,976,984 to Chen et al. describe SRO layers in interconnect processes.

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SUMMARY OF THE INVENTION

Accordingly, it is an object of one or more embodiments of the present invention to provide an improved method of fabricating a damascene structure using an intermediate SRO etch stop layer and/or an uppermost SRO hard mask layer.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a structure having at least one exposed conductive structure is provided. A dielectric barrier layer over the structure and the at least one exposed conductive structure. A lower low-k dielectric layer is formed over the dielectric barrier layer. An upper low-k dielectric layer is formed over the lower low-k dielectric layer. An SRO etch stop layer is formed between the lower low-k dielectric layer and the upper low-k dielectric layer and/or an SRO hard mask layer is formed over the upper low-k dielectric layer. At least the upper and lower low-k dielectric layers are patterned to form the at least one damascene opening exposing at least a portion of the at least one conductive structure, wherein the at least one SRO layer has a high etch selectivity relative to the lower and upper low-k dielectric layers.

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BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 3 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Initial Structure

Fig. 1 illustrates a cross-sectional view of a structure 10 having exposed conductive structures 12 formed therein. Conductive structures 12 may be metal plugs or lines, for example, and may include respective metal barrier layers 14 as shown in the figures. Conductive structures 12 are preferably comprised of copper (Cu), aluminum (Al), tungsten (W) or gold (Au) and are more preferably comprised of copper.

Structure 10 is preferably a silicon substrate and is understood to possibly include a semiconductor wafer or substrate, active and passive devices formed within the wafer, conductive layers and dielectric layers (e.g., inter-poly oxide (IPO), intermetal dielectric (IMD), etc.) formed over the wafer surface. The term "semiconductor structure" is meant to include devices formed within a semiconductor wafer and the layers overlying the wafer.

A dielectric barrier layer 11 is formed over the structure 10 and conductive structures 12 to a thickness of preferably from about 200 to 700Å and more preferably from about 300 to 500Å. Dielectric barrier layer 11 is preferably comprised of SiN, SiON or SiC.

A lower dielectric layer 16 is formed over dielectric barrier layer 11 to a thickness of preferably from about 1500 to 6000Å and more preferably from about

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2500 to 5000Å. Lower dielectric layer 16 is generally an intermetal dielectric (IMD) layer.

Lower dielectric layer 16 is preferably comprised of a low-k dielectric material such as: inorganic low-k dielectrics such as hydrogen silsesquioxane; fluorine (F)-doped or carbon (C)-doped low-k dielectric materials such as FSG, CORAL™manufactured by NVLS; BLACK DIAMOND™manufactured by AMAT; or SiLK™manufactured by Dow Chemical, or other organic low-k materials, for example.

Formation of SRO Etch Stop Layer 18

A silicon-rich (SRO) etch stop layer 18 is formed over the lower dielectric layer 16 to a thickness of preferably from about 200 to 1000Å and more preferably from about 300 to 700Å. SRO etch stop layer 18 will be used as an etch stop for the trench opening in a dual damascene interconnect (and not for the via opening etching).

SRO etch stop layer 18 is preferably formed in an amine-free environment either:

(1) by the reaction of TEOS with O2 using a plasma enhanced chemical vapor deposition (PE CVD) tool under the following conditions:

TEOS gas flow: preferably from about 50 to 2000 mgm and more preferably from about 100 to 1500 mgm;

O_2 gas flow: preferably from about 50 to 2000 sccm and more preferably from about 100 to 1500 sccm;

He gas flow: preferably from about 100 to 5000 sccm and more preferably from about 500 to 3000 sccm;

pressure: preferably from about 2 to 15 Torr and more preferably from about 4 to 7 Torr;

temperature: preferably from about 300 to 450°C and more preferably from about 350 to 400°C;

HF RF power; preferably from about 100 to 1200 W and more preferably from about 200 to 700 W; and

LF RF power; preferably from about 50 to 1000 W and more preferably from about 70 to 500 W;

or

(2) by the reaction of SiH_4 with O_2 using a high density plasma chemical vapor deposition (HDP CVD) tool under the following conditions:

SiH_4 gas flow: preferably from about 20 to 100 sccm and more preferably from about 30 to 50 sccm;

O_2 gas flow: preferably from about 30 to 150 sccm and more preferably from about 40 to 80 sccm;

SiH_4:O_2 ratio: preferably from about 1 : 2 to 1 : 1 and more preferably about 1 : 1.5;

pressure: preferably from about 2 to 7 mTorr and more preferably from about 3 to 6 mTorr;

temperature: preferably from about 250 to 500°C and more preferably from about 300 to 400°C;

LF RF power; preferably from about 2000 to 5000 W and more preferably from about 2500 to 4500 W; and

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bias RF power; preferably from about 0 to 2000 W and more preferably from about 0 to 1000 W.

SRO etch stop layer 18 has a refractive index (RI) of preferably from about 1.52 to 1.75, a dielectric constant (k) of from about 4.0 to 4.2. The Si-rich properties of SRO etch stop layer 18 provide for a much higher film density and greater hardness than other low-k materials which results in a high etch selectivity between SRO etch stop layer 18 and other low-k materials such as lower low-k dielectric layer 16 and upper low-k dielectric layer 20 (see below).

An upper dielectric layer 20 is formed over SRO etch stop layer 18 to a thickness of preferably from about 2000 to 8000Å and more preferably from about 3000 to 6000Å. Upper dielectric layer 20 is generally also an intermetal dielectric (IMD) layer.

Upper dielectric layer 20 is preferably comprised of a low-k dielectric material such as: inorganic low-k dielectrics such as hydrogen silsesquioxane; fluorine (F)-doped or carbon (C)-doped low-k dielectric materials such as FSG, CORAL™manufactured by NVLS; BLACK DIAMOND™manufactured by AMAT; SiLK™manufactured by Dow Chemical or organic low-k materials, for example.

Formation of SRO Hard Mask Layer 22

A silicon-rich (SRO) hard mask layer 22 is formed over the upper dielectric layer 20 to a thickness of preferably from about 200 to 1000Å and more preferably from about 300 to 700Å.

SRO hard mask layer 22 is preferably formed in an amine-free environment by either:

(1) the reaction of TEOS with O_2 using a plasma enhanced chemical vapor deposition (PE CVD) tool under the following conditions:

TEOS gas flow: preferably from about 50 to 2000 mgm and more preferably from about 100 to 1500 mgm;

O_2 gas flow: preferably from about 50 to 2000 sccm and more preferably from about 100 to 1500 sccm;

He gas flow: preferably from about 100 to 5000 sccm and more preferably from about 500 to 3000 sccm;

pressure: preferably from about 2 to 15 Torr and more preferably from about 4 to 7 Torr;

temperature: preferably from about 300 to 450°C and more preferably from about 350 to 400°C;

HF RF power; preferably from about 100 to 1200 W and more preferably from about 200 to 700 W; and

LF RF power; preferably from about 50 to 1000 W and more preferably from about 70 to 500 W;

or

(2) the reaction of SiH_4 with O_2 using a high density plasma chemical vapor deposition (HDP CVD) tool under the following conditions:

SiH_4 gas flow: preferably from about 20 to 100 sccm and more preferably from about 30 to 50 sccm;

O_2 gas flow: preferably from about 30 to 150 sccm and more preferably from about 40 to 80 sccm;

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SiH_4:O_2 ratio: preferably from about 1 : 2 to 1 : 1 and more preferably about 1 : 1.5;

pressure: preferably from about 2 to 7 mTorr and more preferably from about 3 to 6 mTorr;

temperature: preferably from about 250 to 400°C and more preferably from about 300 to 350°C;

LF RF power; preferably from about 2000 to 5000 W; and more preferably from about 2500 to 4500 W; and

bias RF power; preferably from about 0 to 2000 W; and more preferably from about 0 to 1200 W.

SRO hard mask layer 22 has a refractive index (RI) of preferably from about 1.52 to 1.75, a dielectric constant (k) of from about 4.0 to 4.2. The Si-rich properties of SRO hard mask layer 22 provide for a much higher film density and greater hardness than other low-k materials which results in a high etch selectivity between SRO hard mask layer 22 and other low-k materials such as upper low-k dielectric layer 20.

It is noted that under the teachings of the present invention, (1) just an SRO etch stop layer 18 may be formed for dual damascene interconnect formation, (2) just an SRO hard mask layer 22 may be formed; or (3) both an SRO etch stop layer 18 and an SRO hard mask layer 22 may be formed for dual damascene interconnect formation as shown in the figures.

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Patterning of Upper and Lower Dielectric Layers 20, 16

As shown in Fig. 2, the upper and lower dielectric layers 20, 16 are patterned to form for example, via openings 24, 25 and trench openings 26 (only partially shown in Figs. 2 and 3) where via openings 24 and the respective trench openings 26 comprise dual damascene openings 28 (again, only partially shown in Figs. 2 and 3). In the formation of dual damascene openings 28, SRO etch stop layer 18 is used as an etch stop layer only in the formation of trench openings 26.

As shown in Fig. 2, the upper and lower dielectric layers 20, 16 may be patterned using patterned photoresist layer, for example.

Dielectric barrier layer 11 is also patterned to expose at least a portion of conductive structures 12 as shown in Fig. 2.

For example, central via opening 25 is formed through the upper and lower dielectric layers 20, 16. If only via openings 25 were formed, then SRO etch stop layer 18 could be omitted, hence upper and lower dielectric layers 20, 16 could be a single dielectric layer with an overlying SRO hard mask layer 22. Via openings 25 need not be formed central to other openings, such as dual damascene openings 28, and may be the only opening formed, just as dual damascene openings 28 need not be formed distal to any central via opening 25 and may be the only openings formed.

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Formation of Planarized Dual Damascene Structures 36 and Via Structures 38

As shown in Fig. 3, photoresist layer 30 is removed as necessary, and: planarized metal dual damascene structures 36 are formed within dual damascene openings 28; and a planarized via structure, or plug, 38 is formed within central via opening 25 by methods and processes known in the art. Barrier metal layers 32 may be first formed within the dual damascene openings 28 and barrier metal layer 34 may be first formed within the central via opening 25 as shown in Fig. 3.

Planarized metal structures 36, 38 are preferably comprised of copper (Cu), aluminum (Al), tungsten (W) or gold (Au) and are more preferably comprised of copper.

Advantages of the Invention

The advantages of one or more embodiments of the present invention include:

1) formation of damascene structures without masking footing or via poisoning issues;

2) reduction of the effective dielectric constant (k) of intermetal dielectric (IMD) layers;

3) the SRO layers 18, 22 block the moisture absorption by FSG or low-k dielectric films such as IMD layers;

4) the SRO layers 18, 22 block outgassing from FSG or low-k dielectric films such as IMD layers; and

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5) the SRO layers 18, 22 establish a sufficiently high etch selectivity as to FSG or low-k dielectric films such as IMD layers.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.

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CLAIMS

We claim:

1. A method of fabricating at least one damascene opening, comprising steps of:

providing a structure having at least one exposed conductive structure;

forming a dielectric barrier layer over the structure and the at least one exposed conductive structure;

forming a lower low-k dielectric layer over the dielectric barrier layer;

forming an upper low-k dielectric layer over the lower low-k dielectric layer;

forming:

an SRO (silicon-rich oxide) hard mask layer upon the upper low-k dielectric layer

by either a) a reaction of TEOS with O_2 using a PE CVD tool; or b) a reaction of SiH_4 with O_2 using an HDP CVD tool;

and

patterning at least the upper and lower low-k dielectric layers and the dielectric barrier layer to form the at least one damascene opening exposing at least a portion of the at least one exposed conductive structure, wherein the one SRO (silicon-rich oxide) hard mask layer has a high etch selectivity relative to the lower and upper low-k dielectric layers.

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2. The method of claim 1, wherein the structure is a semiconductor substrate; the at least one exposed conductive structure is comprised of Cu, Al, W or Au; and the lower and upper low-k dielectric layers are formed of inorganic low-k materials, F-doped low-k materials, C-doped low-k materials or organic low-k materials.

3. The method of claim 1, wherein the structure is a semiconductor silicon substrate; the at least one exposed conductive structure is comprised of Cu; and the lower and upper low-k dielectric layers are formed of F-doped low-k materials, C-doped low-k materials or organic low-k materials.

4. The method of claim 1, wherein the dielectric barrier layer is from about 200 to 700Å thick, the lower low-k dielectric layer is from about 1500 to 6000Å thick, the upper low-k dielectric layer is from about 2000 to 8000Å thick and the SRO hard mask layer formed is from about 200 to 1000Å thick.

5. The method of claim 1, wherein the dielectric barrier layer is from about 300 to 500Å thick, the lower low-k dielectric layer is from about 2500 to 5000Å thick, the upper low-k dielectric layer is from about 3000 to 6000Å thick, and the SRO hard mask layer formed is from about 300 to 700Å thick.

6. The method of claim 1, wherein any SRO etch stop layer and any SRO hard mask layer are each formed under the following conditions using the PE CVD tool:

TEOS gas flow: from about 50 to 2000 mgm;

O_2 gas flow: from about 50 to 2000 mgm;

He gas flow: from about 100 to 5000 sccm;

pressure: from about 2 to 15 Torr;

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temperature: from about 300 to 450°C;

HF RF power: from about 100 to 1200 W; and

LF RF power: from about 50 to 1000 W.

7. The method of claim 1, wherein the SRO hard mask layer is formed under the following conditions using the PE CVD tool:

TEOS gas flow: from about 100 to 1500 mgm;

O_2 gas flow: from about 100 to 1500 mgm;

He gas flow: from about 500 to 3000 sccm;

pressure: from about 4 to 7 Torr;

temperature: from about 350 to 400°C;

HF RF power: from about 200 to 700 W; and

LF RF power: from about 70 to 500 W.

8. The method of claim 1, wherein the dielectric barrier layer is comprised of SiN, SiON or SiC.

9. The method of claim 1, wherein any SRO etch stop layer and any SRO hard mask layer formed each have a refractive index of from about 1.52 to 1.75.

10. A method of fabricating at least one damascene opening, comprising steps of:

providing a structure having at least one exposed conductive structure;

forming a dielectric barrier layer over the structure and the at least one exposed conductive structure;

forming a lower low-k dielectric layer over the dielectric barrier layer;

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forming an SRO (silicon-rich oxide) etch stop layer over the lower low-k dielectric layer by a) a reaction of TEOS with O_2 using a PE CVD tool; or b) a reaction of SiH_4 with O_2 using the HDP CVD tool;

forming an upper low-k dielectric layer over the SRO (silicon-rich oxide) etch stop layer;

forming an SRO (silicon-rich oxide) hard mask layer upon the upper low-k dielectric layer by a) the reaction of TEOS with O_2 using the PE CVD tool; or b) the reaction of SiH_4 with O_2 using the HDP CVD tool;

and

patterning at least the upper and lower low-k dielectric layers to form the at least one damascene opening exposing at least a portion of the at least one exposed conductive structure, wherein the SRO (silicon-rich oxide) etch stop layer and the SRO (silicon-rich oxide) hard mask each have a high etch selectivity relative to the lower and upper low-k dielectric layers.

11. The method of claim 10, wherein the structure is a semiconductor substrate; the at least one exposed conductive structure is comprised of Cu, Al, W or Au; and the lower and upper low-k dielectric layers are formed of inorganic low-k materials, F-doped low-k materials, C-doped low-k materials or organic low-k materials.

12. The method of claim 10, wherein the structure is a semiconductor silicon substrate; the at least one exposed conductive structure is comprised of Cu; and the lower and upper low-k dielectric layers are formed of F-doped low-k materials, C-doped low-k materials or organic low-k materials.

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13. The method of claim 10, wherein the dielectric barrier layer is from about 200 to 700Å thick, the lower low-k dielectric layer is from about 1500 to 6000Å thick, the upper low-k dielectric layer is from about 2000 to 8000Å thick, the SRO etch stop layer is from about 200 to 1000Å thick and the SRO hard mask layer is from about 200 to 1000Å thick.

14. The method of claim 10, wherein the dielectric barrier layer is from about 300 to 500Å thick, the lower low-k dielectric layer is from about 2500 to 5000Å thick, the upper low-k dielectric layer is from about 3000 to 6000Å thick, the SRO etch stop layer is from about 300 to 700Å thick and the SRO hard mask layer is from about 300 to 700Å thick.

15. The method of claim 10, wherein the SRO etch stop layer and the SRO hard mask layer are each formed under the following conditions using the PE CVD tool:

TEOS gas flow: from about 50 to 2000 mgm;

O_2 gas flow: from about 50 to 2000 mgm;

He gas flow: from about 100 to 5000 sccm;

pressure: from about 2 to 15 Torr;

temperature: from about 300 to 450°C;

HF RF power: from about 100 to 1200 W; and

LF RF power: from about 50 to 1000 W.

16. The method of claim 10, wherein the SRO etch stop layer and the SRO hard mask layer are each formed under the following conditions using the PE CVD tool:

TEOS gas flow: from about 100 to 1500 mgm;

O_2 gas flow: from about 100 to 1500 mgm;

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He gas flow: from about 500 to 3000 sccm;

pressure: from about 4 to 7 Torr;

temperature: from about 350 to 400°C;

HF RF power: from about 200 to 700 W; and

LF RF power: from about 70 to 500 W.

17. The method of claim 10, wherein the SRO etch stop layer and the SRO hard mask layer have an refractive index of from about 1.52 to 1.75.

18. A method of fabricating at least one damascene opening, comprising steps of:

providing a semiconductor substrate having at least one exposed copper structure;

forming a dielectric barrier layer over the semiconductor substrate and the at least one exposed copper structure;

forming a lower low-k dielectric layer over the dielectric barrier layer;

forming an SRO (silicon-rich oxide) etch stop layer over the lower low-k dielectric layer wherein the SRO (silicon-rich oxide) etch stop layer being formed by a) a reaction of TEOS with O_2 using a PE CVD tool; or b) a reaction of SiH_4 with O_2 using an HDP CVD tool;

forming an upper low-k dielectric layer over the SRO (silicon-rich oxide) etch stop layer;

forming an SRO (silicon-rich oxide) hard mask layer upon the upper low-k dielectric layer wherein the SRO (silicon-rich oxide) hard mask layer being formed by a) the reaction of TEOS with O_2 using the PE CVD tool; or b) the reaction of SiH_4 with O_2 using the HDP CVD tool;

and

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patterning at least the upper and lower low-k dielectric layers to form the at least one damascene opening exposing at least a portion of the at least one exposed copper structure, wherein the SRO (silicon-rich oxide) etch stop layer and the SRO (silicon-rich oxide) hard mask each have a high etch selectivity relative to the lower and upper low-k dielectric layers.

19. The method of claim 18, wherein the lower and upper low-k dielectric layers are formed of inorganic low-k materials, F-doped low-k materials, C-doped low-k materials or organic low-k materials.

20. The method of claim 18, wherein the dielectric barrier layer is from about 200 to 700Å thick, the lower low-k dielectric layer is from about 1500 to 6000Å thick, the upper low-k dielectric layer is from about 2000 to 8000Å thick, the SRO etch stop layer is from about 200 to 1000Å thick and the SRO hard mask layer is from about 200 to 1000Å thick.

21. The method of claim 18, wherein the dielectric barrier layer is from about 300 to 500Å thick, the lower low-k dielectric layer is from about 2500 to 5000Å thick, the upper low-k dielectric layer is from about 3000 to 6000Å thick, the SRO etch stop layer is from about 300 to 700Å thick and the SRO hard mask layer is from about 300 to 700Å thick.

22. The method of claim 18, wherein the SRO etch stop layer and the SRO hard mask layer are each formed under the following conditions using the PE CVD tool:

TEOS gas flow: from about 50 to 2000 mgm;

O_2 gas flow: from about 50 to 2000 mgm;

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He gas flow: from about 100 to 5000 sccm;

pressure: from about 2 to 15 Torr;

temperature: from about 300 to 450°C;

HF RF power: from about 100 to 1200 W; and

LF RF power: from about 50 to 1000 W.

23. The method of claim 18, wherein the SRO etch stop layer and the SRO hard mask layer are each formed under the following conditions using the PE CVD tool:

TEOS gas flow: from about 100 to 1500 mgm;

O_2 gas flow: from about 100 to 1500 mgm;

He gas flow: from about 500 to 3000 sccm;

pressure: from about 4 to 7 Torr;

temperature: from about 350 to 400°C;

HF RF power: from about 200 to 700 W; and

LF RF power: from about 70 to 500 W.

24. The method of claim 18, wherein the SRO etch stop later and the SRO hard mask layer have a refractive index of from about 1.52 to 1.75.

25. The method of claim 18, including a step of forming at least one planarized metal damascene structure within the at least one damascene opening.

26. The method of claim 18, including a step of forming at least one planarized copper damascene structure within the at least one damascene opening.

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27. The method of claim 18, wherein the at least one damascene opening is a dual damascene opening; and including a step of forming at least one planarized metal dual damascene structure within the at least one dual damascene opening.