Claims

1. A programmable logic unit, comprising:

one or more programmable processing elements; and

a sequencer selecting one interpretation register from multiple interpretation registers based on a Type ID value within instructions in an instruction stream, obtaining one instruction group from multiple instruction groups based on the value of the selected interpretation register, determining command from the obtained instruction group based on an opcode value within the instructions, and sending commands to said processing elements,

wherein values of each interpretation register can be updated by executing the instructions and same operations operating on a different operand data format are defined in the same opcode positions within at least two different instruction groups within the multiple instruction groups.

2. The unit of Claim 1, wherein said instruction stream includes both processing instructions and also sequencing instructions.

3. The unit of Claim 1, wherein said instruction stream includes both processing instructions and also sequencing instructions, and wherein both said processing instructions and said sequencing instructions include said Type ID, and wherein said Type ID also indicates whether each instruction is a processing instruction or a sequencing instruction.

4. The unit of Claim 1, wherein said instruction stream includes both processing instructions and also sequencing instructions, and said sequencing instructions can include commands for changing the values in at least some ones of said interpretation registers.

5. The unit of Claim 1, wherein said commands are expanded by at least one said sequencer; and wherein said instruction stream includes both processing instructions and also sequencing instructions; and wherein said sequencing instructions can include set-up

commands which are executed by said sequencer and not by said processing elements, including commands for changing the values in the interpretation register.

6. The unit of Claim 1, wherein said commands are expanded by at least one said sequencer; and wherein said sequencer broadcasts a single instruction stream to multiple processing elements in a SIMD configuration,

7. The unit of Claim 1, wherein each single one of said instructions specifies only a single opcode.

8. The unit of any one of Claims 2-5, wherein each said processing instruction includes an index number which selects a respective portion of said interpretation registers, and wherein said sequencer expands said respective processing instruction by using said respective portion of said interpretation registers.

9. A method of executing an instruction stream on a logic unit comprising one or more programmable processing elements and at least one sequencer, comprising the actions of:

a) interpreting, by said sequencer, each of the instructions, by selecting one interpretation register from multiple interpretation registers based on a Type ID field of each instruction in the instruction stream, by obtaining one instruction group from multiple instruction groups based on the value of the selected interpretation register, and by determining command from the obtained instruction group based on an opcode field of each instruction, and sending said command to said processing elements; and

b) executing said instructions in accordance with said step (a),

wherein values of each interpretation register can be updated by executing the instructions and same operations operating on a different operand data format are defined in the same opcode positions within at least two different instruction groups within the multiple instruction groups.

10. The method of Claim 9, wherein said instruction stream includes both processing instructions and also sequencing instructions.

11. The method of Claim 9, wherein said instruction stream includes both processing instructions and also sequencing instructions, and wherein said Type ID also indicates whether each instruction is a processing instruction or a sequencing instruction.

12. The method of Claim 9, wherein said instruction stream includes both processing instructions and also sequencing instructions, and said sequencing instructions can include commands for changing the values in at least some ones of said interpretation registers.

13. The method of Claim 9, wherein said commands are expanded by said at least one sequencer; and wherein said instruction stream includes both processing instructions and also sequencing instructions; and wherein said sequencing instructions can include set-up commands which are executed by said sequencer and not by said processing elements, including commands for changing the values in the interpretation register.

14. The method of Claim 9, wherein said commands are expanded by said at least one sequencer; and wherein said sequencer broadcasts a single instruction stream to multiple said processing elements in a SIMD configuration.

15. The method of Claim 9, wherein each said instruction specifies only a single opcode.

16. The method of any one of Claims 10-13, wherein each said processing instruction includes an index number which selects a respective particular portion of said interpretation register, and wherein said sequencer expands said respective processing instruction by using said respective particular portion of said interpretation register.

17. A method for executing a series of processing instructions, comprising the actions of:

a) interpreting each of the instructions, by selecting one interpretation register from multiple interpretation registers based on a Type ID field of each instruction in the series of processing instructions, by obtaining one instruction group from multiple instruction groups based on the value of the selected interpretation register, and by determining command from the obtained instruction group based on an opcode field of each instruction; wherein said Type ID field distinguishes between sequencer and processing-element instructions, and also distinguishes among multiple different formats for processing-element instructions; and

b) executing said instructions in accordance with said step (a),

wherein values of each interpretation register can be updated by executing the instructions and same operations operating on a different operand data format are defined in the same opcode positions within at least two different instruction groups within the multiple instruction groups.

18. The method of Claim 17, wherein said sequencer instructions can include commands for changing the values in at least some ones of said interpretation registers.

19. The method of Claim 17, wherein said commands are expanded by at least one sequencer; and wherein said sequencer instructions can include set-up commands which are executed only by said sequencer.

20. The method of Claim 17, wherein said sequencer instructions can include commands for changing the values in the interpretation register.

21. The method of Claim 17, wherein said commands are expanded by at least one sequencer; and wherein said sequencer broadcasts a single instruction stream to multiple processing elements in a SIMD configuration.

22. The method of Claim 17, wherein each single said processing instruction specifies only a single opcode.

23. A computing architecture in which: processing instructions in an instruction stream, each including both an opcode and also a Type ID which selects among multiple interpretation registers;

some of said interpretation registers containing information for interpreting said commands differently, depending on which of said interpretation registers has been selected; and

sequencing logic which is connected to send an instruction to one or more processing elements, the instruction being generated by selecting one interpretation register from multiple interpretation registers based on the value of the Type ID, by obtaining one instruction group from multiple instruction groups based on information stored in said selected interpretation registers, and by determining command from the obtained instruction group based on the value of the opcode,

wherein values of each interpretation register can be updated by executing the instructions and same operations operating on a different operand data format are defined in the same opcode positions within at least two different instruction groups within the multiple instruction groups.

24. The architecture of Claim 23, wherein said instruction stream includes both said processing instructions and also sequencing instructions which are executed by said sequencing logic.

25. The architecture of Claim 23, wherein said instruction stream includes both said processing instructions and also sequencing instructions, and both said processing instructions and said sequencing instructions include said Type ID, and said Type ID also indicates whether each instruction is a processing instruction or a sequencing instruction.

26. The architecture of Claim 23, wherein said instruction stream includes both said processing instructions and also sequencing instructions, and the sequencing instructions can include commands for changing the values in the interpretation register.

27. The architecture of Claim 23, wherein said instruction stream includes both said processing instructions and also sequencing instructions which cause said sequencing logic to change the values in the interpretation register.

28. The architecture of Claim 23, wherein said sequencing logic broadcasts a single instruction stream to multiple processing elements in a SIMD configuration.

29. The architecture of Claim 23, wherein each said processing instruction includes only one op code.

30. A computing architecture in which:

processing instructions are mixed with sequencing instructions in a stream, each instruction comprising a Type ID and an opcode; and

at least one sequencer is connected to receive the processing instructions, to select one interpretation register from multiple interpretation registers based on the Type ID value, to obtain one instruction group from multiple instruction groups based on the value of the selected interpretation register, and to determine command from the obtained instruction group based on the opcode value, in order to produce executable commands for one or more processing elements; and

said sequencer is also connected to receive the sequencing instructions, and can change the values in said interpretation register in response to at least one said sequencing instruction,

wherein same operations operating on a different operand data format are defined in the same opcode positions within at least two different instruction groups within the multiple instruction groups.

31. The architecture of Claim 30, wherein said instruction stream includes both said processing instructions and also sequencing instructions, and both said processing instructions and said sequencing instructions include said Type ID, and said Type ID also indicates

whether each instruction is a processing instruction or a sequencing instruction.

32. The architecture of Claim 30, wherein said sequencer broadcasts a single instruction stream to multiple processing elements in a SIMD configuration.

33. The architecture of Claim 30, wherein each said processing instruction includes only one opcode.

34. A multiprocessing system, comprising multiple interconnected units according to Claim 1.

CLAIMS

What is claimed is:

1. A programmable logic unit, comprising:

one or more programmable processing elements; and

a sequencer which is connected to decode instructions in an instruction stream using indirect reference to multiple interpretation registers, as specified by a Type ID value within said instructions, and to send commands to said processing elements accordingly.

2. The unit of Claim 1, wherein said instruction stream includes both processing instructions and also sequencing instructions.

3. The unit of Claim 1, wherein said instruction stream includes both processing instructions and also sequencing instructions, and wherein both said processing instructions and said sequencing instructions include said Type ID, and wherein said Type ID also indicates whether each instruction is a processing instruction or a sequencing instruction.

4. The unit of Claim 1, wherein said instruction stream includes both processing instructions and also sequencing instructions, and said sequencing instructions can include commands for changing the values in at least some ones of said interpretation registers.

5. The unit of Claim 1, wherein said commands are expanded by at least one said sequencer; and wherein said instruction stream includes both processing instructions and also sequencing instructions; and wherein said sequencing instructions can include set-up commands which are executed by said sequencer and not by said processing elements, including commands for changing the values in the interpretation register.

6. The unit of Claim 1, wherein said commands are expanded by at least one said sequencer; and wherein said sequencer broadcasts a single instruction stream to multiple processing elements in a SIMD configuration.

7. The unit of Claim 1, wherein each single one of said instructions specifies only a single opcode.

8. The unit of Claim 1, wherein each said processing instruction includes an index number which selects a respective portion of said interpretation registers, and wherein said sequencer expands said respective processing instruction by using said respective portion of said interpretation registers.

9. A method of executing a series of processing instructions, comprising the actions of:

a) interpreting each of the instructions with reference to a respective interpretation register which is specified in a Type ID field of ones of said instructions; and

b) executing said instructions in accordance with said step (a).

10. The method of Claim 9, wherein said instruction stream includes both processing instructions and also sequencing instructions.

11. The method of Claim 9, wherein said instruction stream includes both processing instructions and also sequencing instructions, and wherein said Type ID also indicates whether each instruction is a processing instruction or a sequencing instruction.

12. The method of Claim 9, wherein said instruction stream includes both processing instructions and also sequencing instructions, and said sequencing instructions can include commands for changing the values in at least some ones of said interpretation registers.

13. The method of Claim 9, wherein said commands are expanded by at least one sequencer; and wherein said instruction stream includes both processing instructions and also sequencing instructions; and wherein said sequencing instructions can include set-up commands which are executed by said sequencer and not by said processing elements, including commands for changing the values in the interpretation register.

14. The method of Claim 9, wherein said commands are expanded by at least one sequencer; and wherein said sequencer broadcasts a single instruction stream to multiple processing elements in a SIMD configuration.

15. The method of Claim 9, wherein said command bits of each single processing instruction specify only a single opcode.

16. The method of Claim 9, wherein each said processing instruction includes an index number which selects a respective particular portion of said interpretation register, and wherein said sequencer expands said respective processing instruction by using said respective particular portion of said interpretation register.

17. A method for executing a series of processing instructions, comprising the actions of:

a) interpreting each of the instructions using an indirect reference to a respective interpretation register which is specified in a Type ID field of ones of said instructions; wherein said Type ID field distinguishes between sequencer and processing-element instructions, and also distinguishes among multiple different formats for processing-element instructions; and

b) executing said instructions in accordance with said step (a).

18. The method of Claim 17, wherein said sequencer instructions can include commands for changing the values in at least some ones of said interpretation registers.

19. The method of Claim 17, wherein said commands are expanded by at least one sequencer; and wherein said sequencer instructions can include set-up commands which are executed only by said sequencer.

20. The method of Claim 17, wherein said sequencer instructions can include commands for changing the values in the interpretation register.

21. The method of Claim 17, wherein said commands are expanded by at least one sequencer; and wherein said sequencer broadcasts a single instruction stream to multiple processing elements in a SIMD configuration.

22. The method of Claim 17, wherein each single said processing instruction specifies only a single opcode.

23. A computing architecture in which:

processing instructions in an instruction stream, each including both command bits and also a Type ID which selects among multiple interpretation registers;

some of said interpretation registers containing information for interpreting said commands differently, depending on which of said interpretation registers has been selected; and

sequencing logic which is connected to expand said commands, in combination with information stored in said interpretation registers, to thereby generate an expanded instruction which is sent to one or more processing elements.

24. The architecture of Claim 23, wherein said instruction stream includes both said processing instructions and also sequencing instructions which are executed by said sequencing logic.

25. The architecture of Claim 23, wherein said instruction stream includes both said processing instructions and also sequencing instructions, and both said processing instructions and said sequencing instructions include said Type ID, and said Type ID also indicates whether each instruction is a processing instruction or a sequencing instruction.

26. The architecture of Claim 23, wherein said instruction stream includes both said processing instructions and also sequencing instructions, and the sequencing instructions can include commands for changing the values in the interpretation register.

27. The architecture of Claim 23, wherein said instruction stream includes both said processing instructions and also sequencing instructions which cause said sequencing logic to change the values in the interpretation register.

28. The architecture of Claim 23, wherein said sequencing element broadcasts a single instruction stream to multiple processing elements in a SIMD configuration.

29. The architecture of Claim 23, wherein each said processing instruction includes only one op code.

30. A computing architecture in which:

processing instructions are mixed with sequencing instructions in a stream; and

at least one sequencer is connected to receive the processing instructions, and to expand at least some of the processing instructions by use of an interpretation register to produce executable commands for one or more processing elements; and

said sequencer is also connected to receive the sequencing instructions, and can change the values in said interpretation register in response to at least one said sequencing instruction.

31. The architecture of Claim 30, wherein said instruction stream includes both said processing instructions and also sequencing instructions, and both said processing instructions and said sequencing instructions include said Type ID, and said Type ID also indicates whether each instruction is a processing instruction or a sequencing instruction.

32. The architecture of Claim 30, wherein said sequencer broadcasts a single instruction stream to multiple processing elements in a SIMD configuration.

33. The architecture of Claim 30, wherein each said processing instruction includes only one opcode.

34. A multiprocessing system, comprising multiple interconnected units according to Claim 1.