CLAIMS

1. A virtual ground sensing circuit, comprising:

an operational amplifier comprising a non-inverting input, an inverting input, and an amplifier output;

a follower circuit including an n-MOS transistor and a p-MOS transistor, an input of the follower circuit including a gate of the n-MOS transistor operably coupled to a gate of the p-MOS transistor, and an output of the follower circuit including a source of the n-MOS transistor operably coupled to a source of the p-MOS transistor, the output of the follower circuit operably coupled to the inverting input of the operational amplifier;

a comparator configured to compare a sense node voltage at a drain of one of the n-MOS transistor and the p-MOS transistor to a reference voltage potential; and

another comparator configured to compare another sense node voltage at a drain of the other of the n-MOS transistor and the p-MOS transistor to another reference voltage potential.

2. The virtual ground sensing circuit of claim 1, wherein a drain of the other of the n-MOS transistor and the p-MOS transistor is operably coupled to a power supply voltage potential.

3. The virtual ground sensing circuit of claim 1, wherein the drain of the one of the n-MOS transistor and the p-MOS transistor is operably coupled to a power supply voltage potential through a transistor configured to isolate the drain of the one of the n-MOS transistor and the p-MOS transistor from the power supply voltage potential during a sense operation.

4. The virtual ground sensing circuit of claim 1, wherein the output of the follower circuit is operably coupled to a conductive line decoder configured to selectively operably couple the output of the follower circuit to one of a plurality of conductive lines of a memory cell array.

5. The virtual ground sensing circuit of claim 1, wherein the comparator is configured to compare a drain voltage potential of the p-MOS transistor to the reference voltage potential.

6. The virtual ground sensing circuit of claim 1, wherein the sense node has a sense node capacitance.

7. The virtual ground sensing circuit of claim 6, wherein the sense node capacitance includes a parasitic capacitance.

8. The virtual ground sensing circuit of claim 1, further comprising a digital to analog converter (DAC) configured to provide the reference voltage potential to the comparator, wherein a multi-bit digital signal swept from a low digital value to a high digital value is applied to an input of the DAC during a sense operation.

9. The virtual ground sensing circuit of claim 8, further comprising a latch network configured to store a digital value of the multi-bit digital signal that corresponds to a data state of a selected memory cell operably coupled to the conductive line.

10. The virtual ground sensing circuit of claim 9, wherein the latch network is configured to be clocked by an output of the comparator.

11. The virtual ground sensing circuit of claim 1, wherein the operational amplifier is an operational transconductance amplifier.

12. An electrical system, comprising:

at least one memory cell; and

control circuitry operably coupled to the at least one memory cell, the control circuitry comprising:

an operational amplifier comprising a non-inverting input, an inverting input, and an amplifier output;

a follower circuit comprising a first transistor and a second transistor, an input of the follower circuit comprising a gate of the first transistor operably coupled to a gate of the second transistor, and an output of the follower circuit comprising a source of the first transistor operably coupled to a source of the second transistor, the output of the follower circuit operably coupled to the inverting input of the operational amplifier;

a comparator configured to compare a sense node voltage at a drain of one of the first transistor and the second transistor to a reference voltage potential; and

another comparator configured to compare another sense node voltage at a drain of the other of the first transistor and the second transistor to another reference voltage potential.

13. The electrical system of claim 12, wherein the control circuitry further comprises a feedback circuit operably coupling the output of the comparator circuit to the inverting input of the operational amplifier and to a conductive line.

14. The electrical system of claim 13, further comprises the conductive line operably coupled to the at least one memory cell.

15. The electrical circuit of claim 12, further comprising a digital to analog converter (DAC) configured to receive a digital signal, an output of the DAC operably coupled to an inverting input of the comparator.