

FIG. 1A

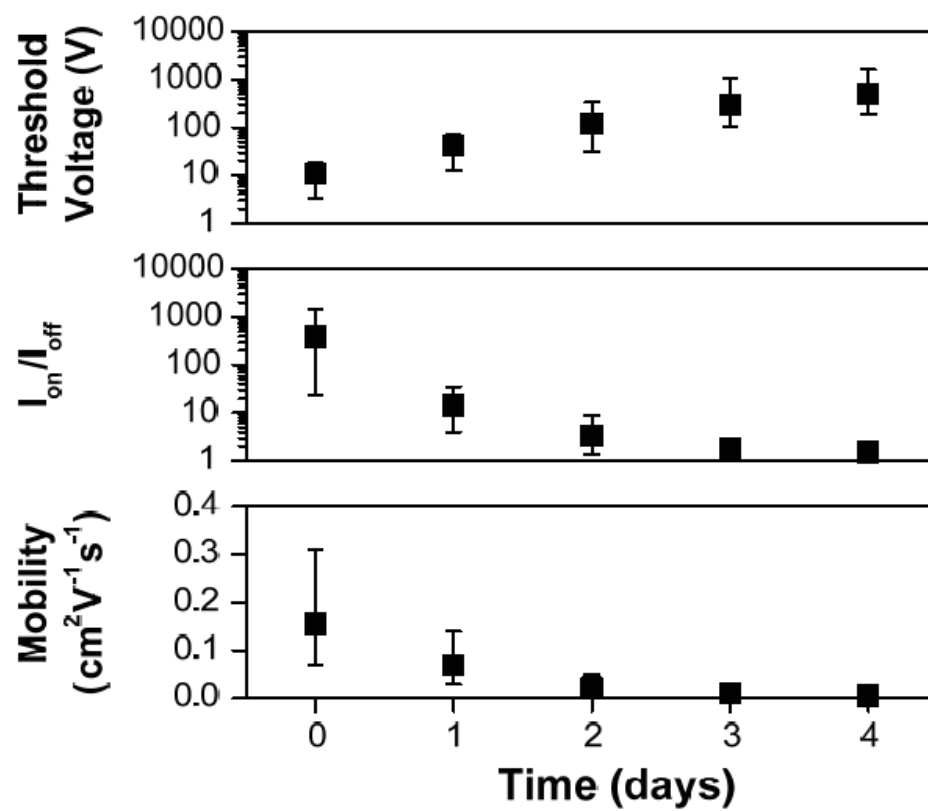
100a

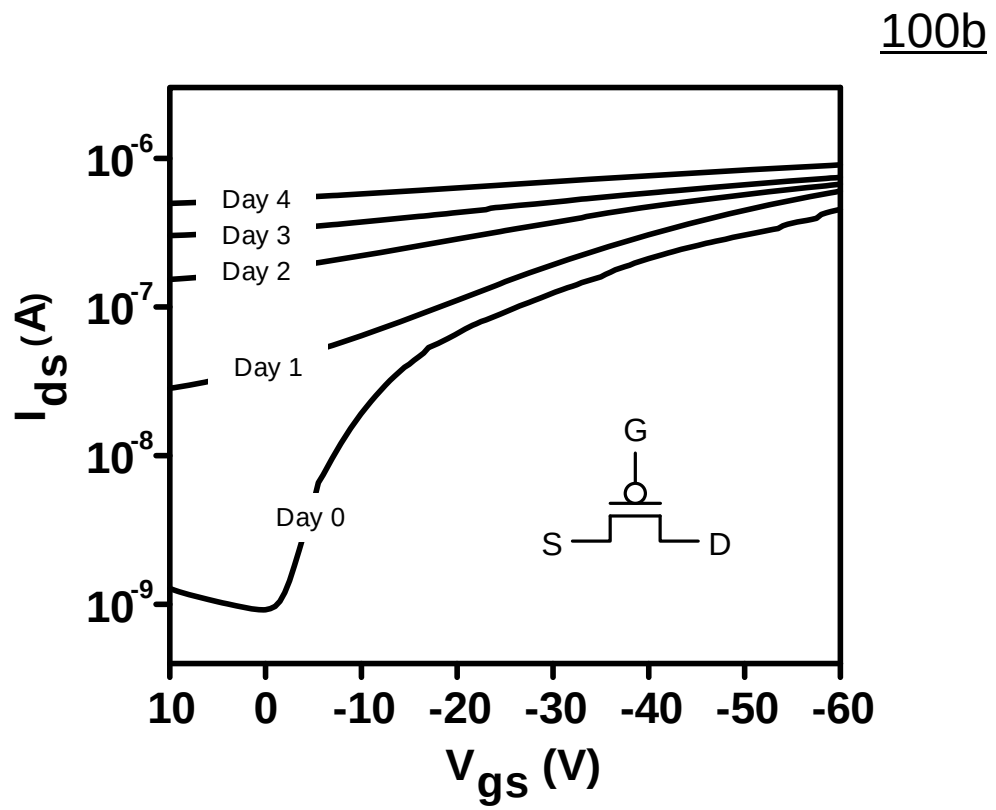
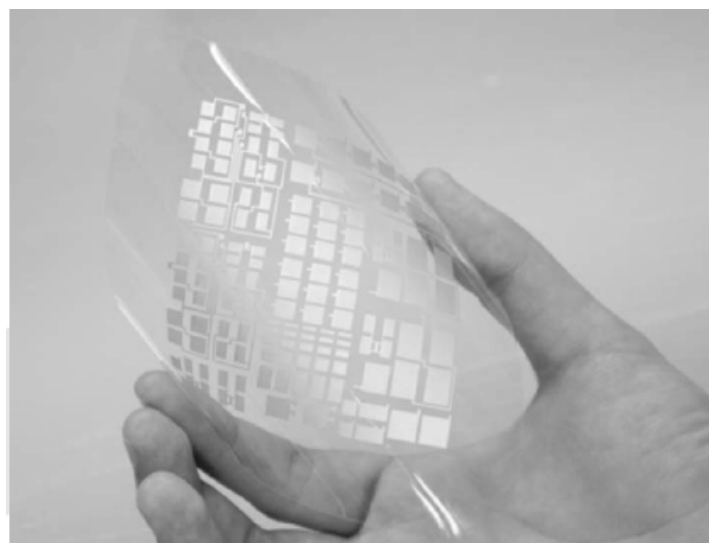
FIG. 1B**FIG. 1C**

FIG. 1D

100d

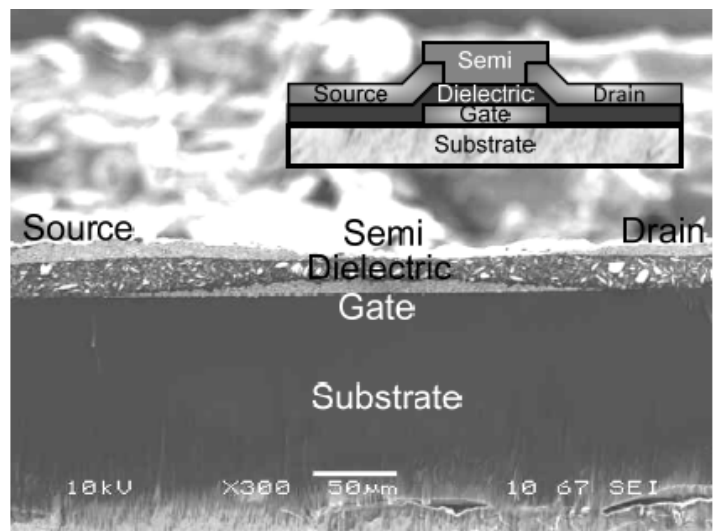
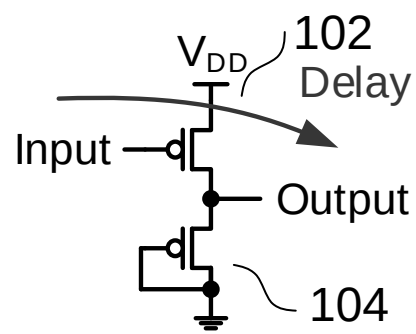


FIG. 1E

100e



Circuit

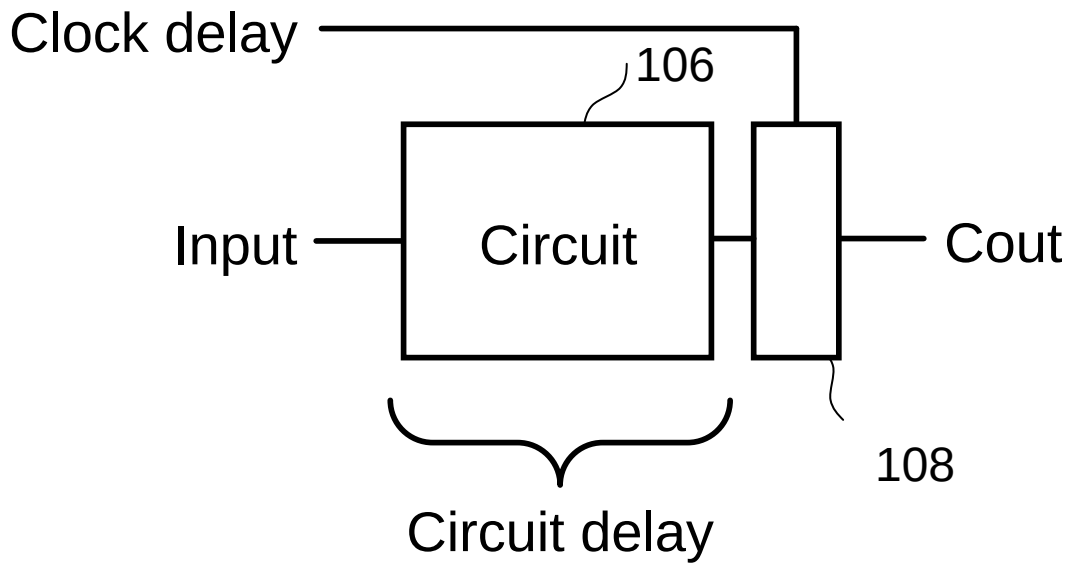
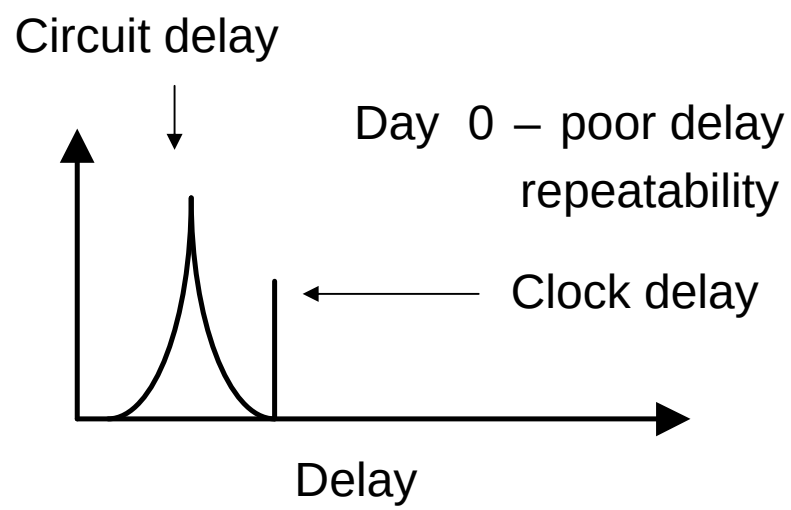
FIG. 1F100f**FIG. 1G**100g

FIG. 1H

100h

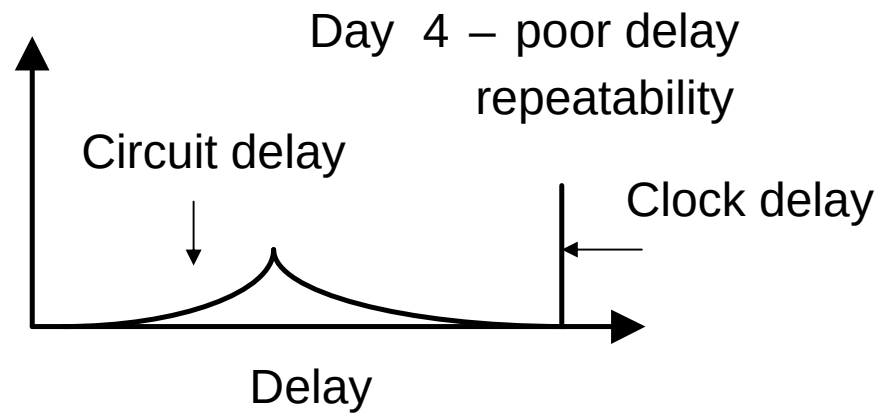


FIG. 2

200

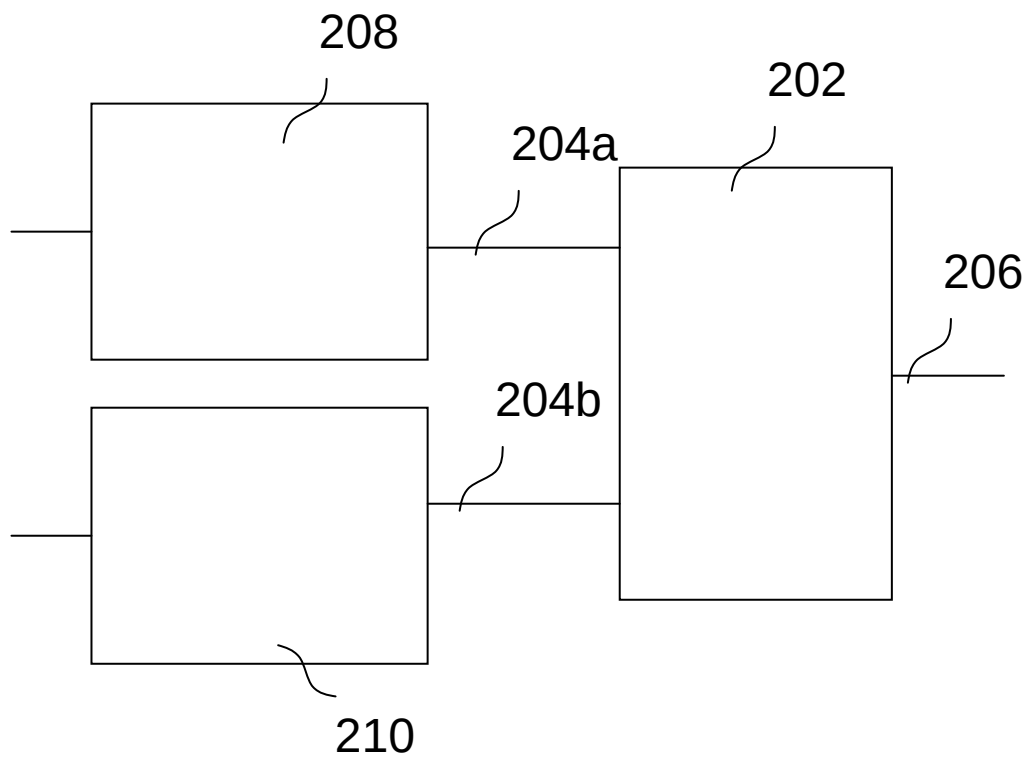


FIG. 3

300

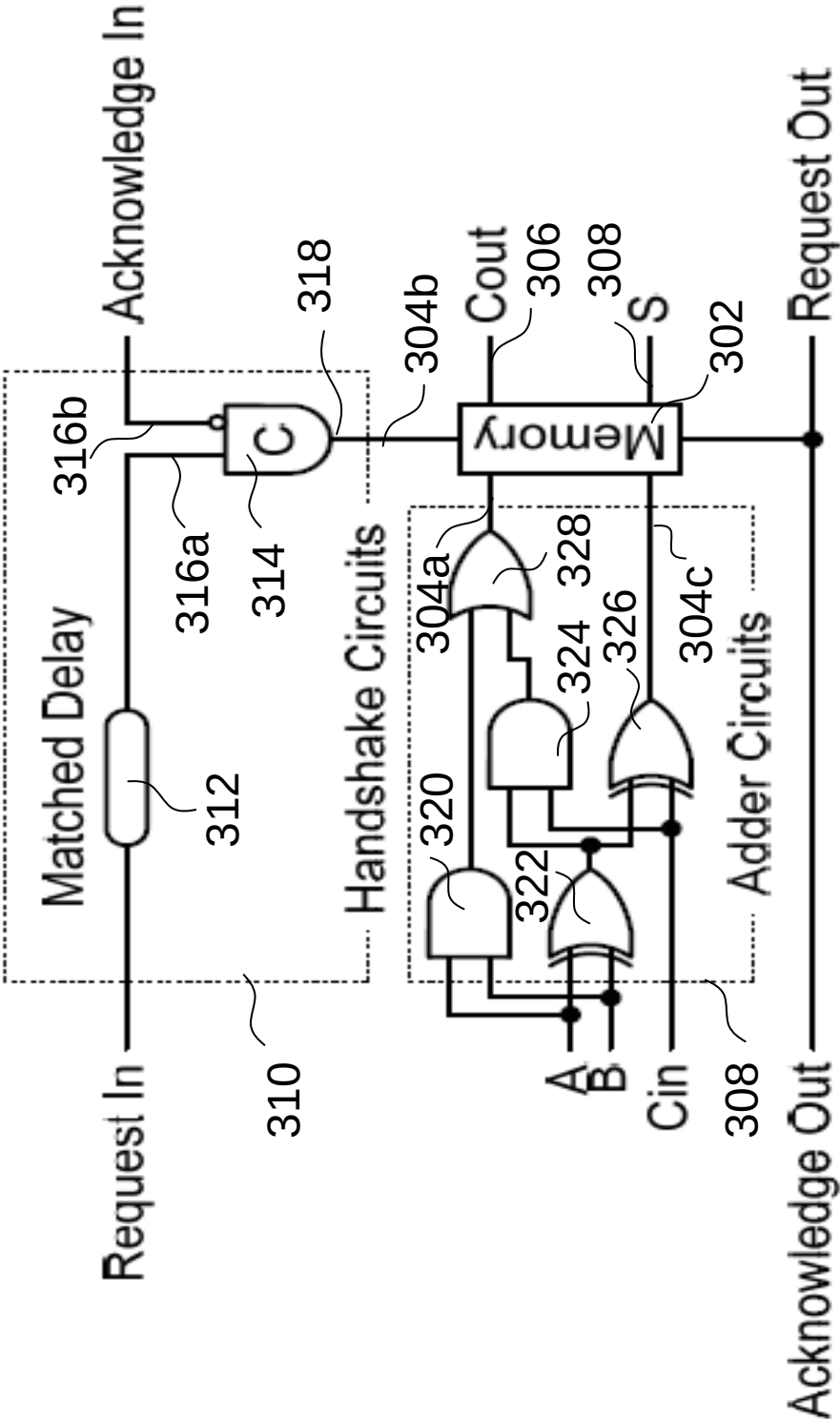
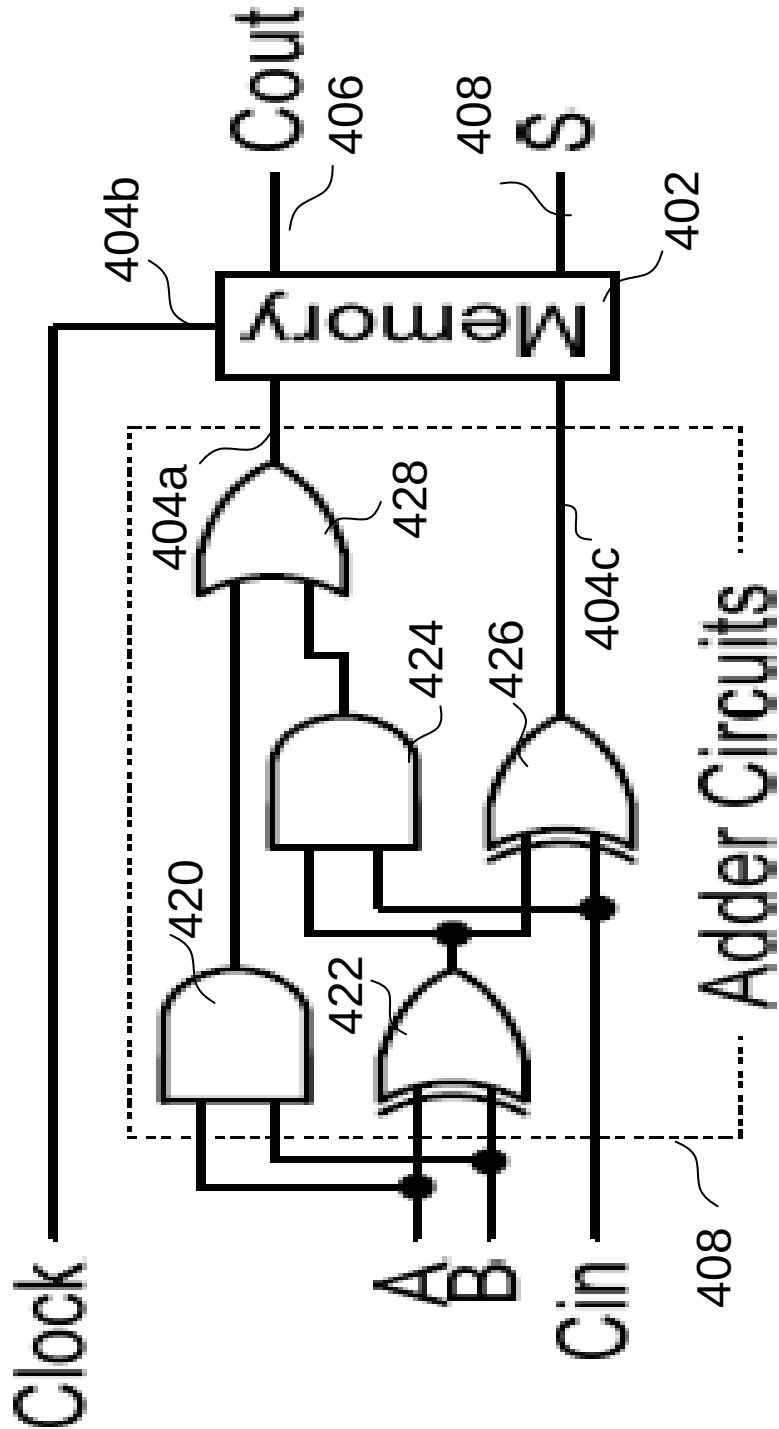


FIG. 4

400



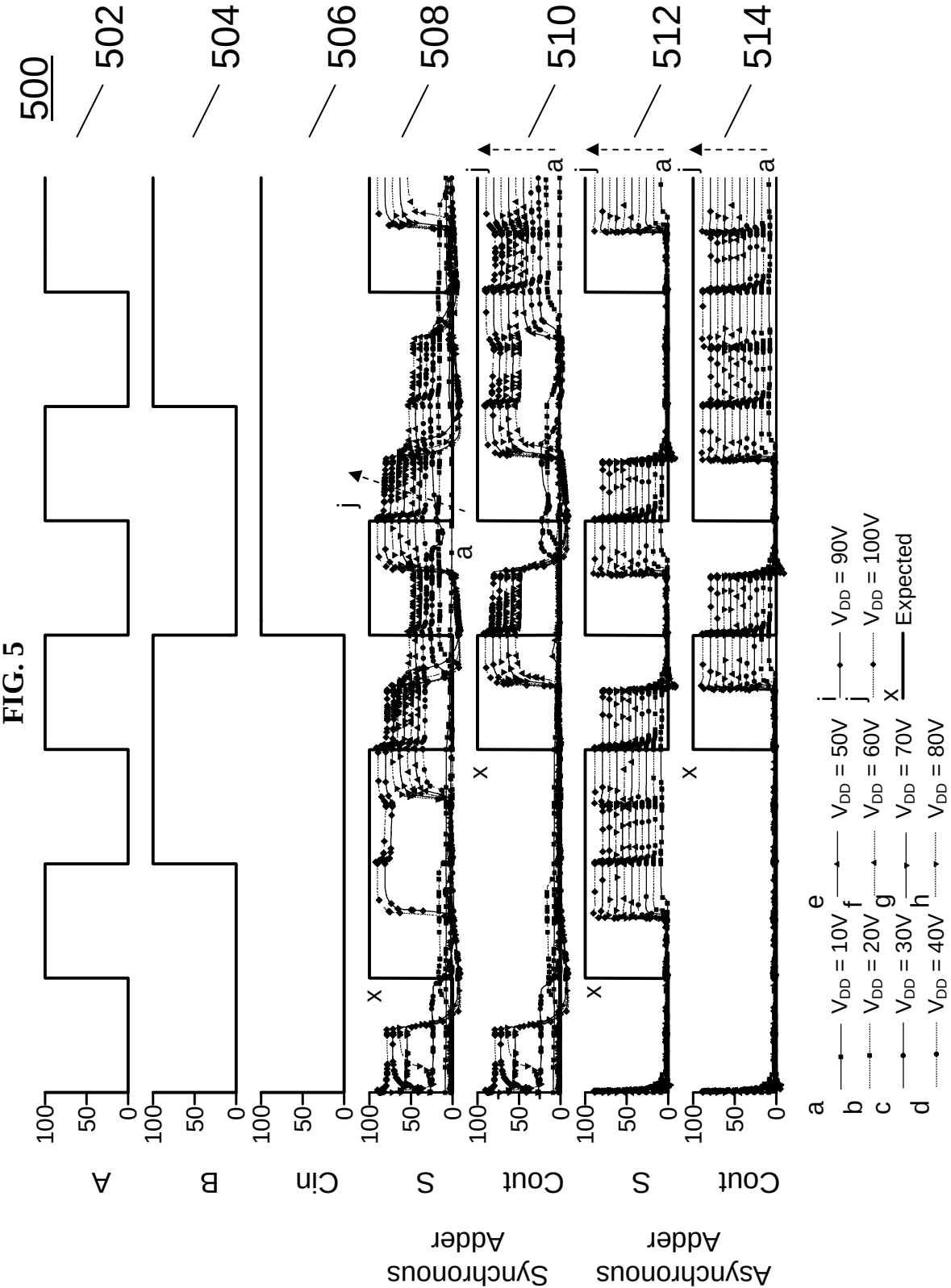
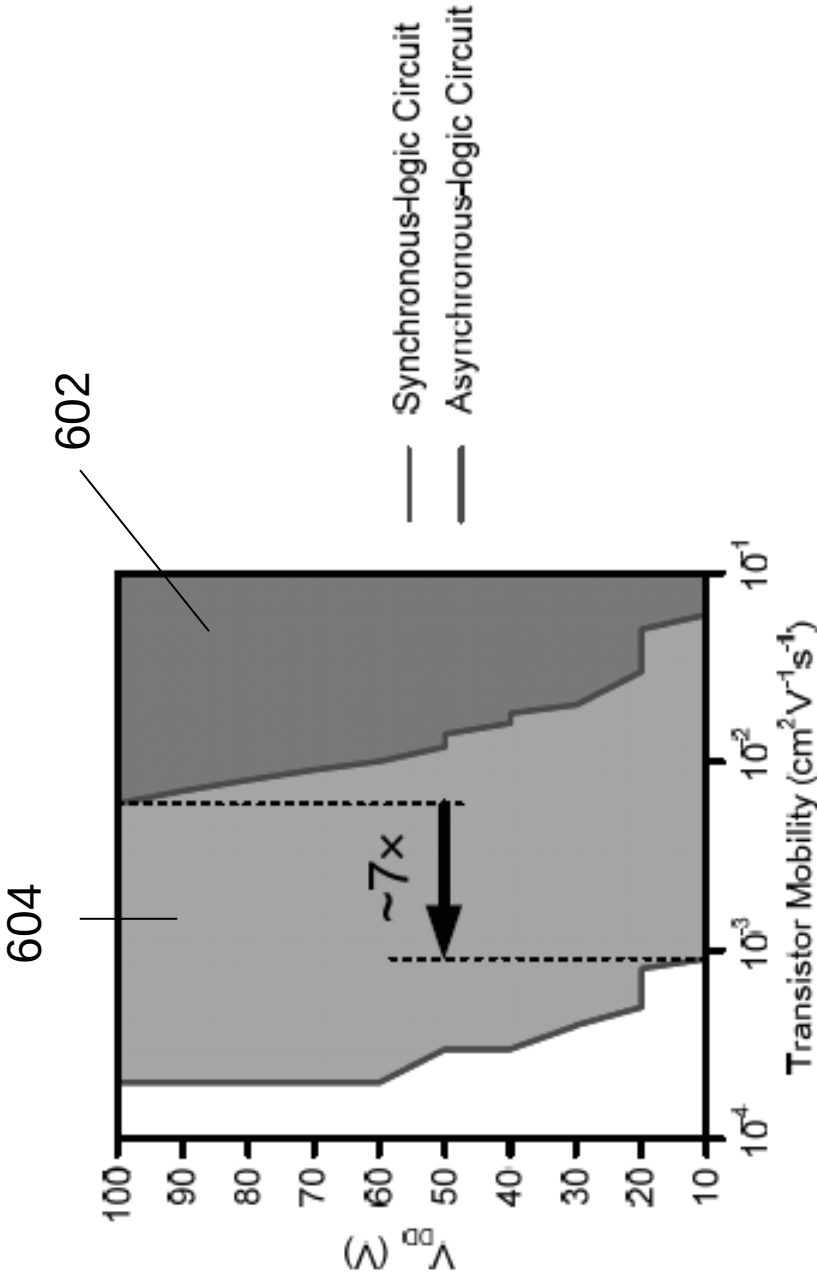


FIG. 6

600



604

602

Synchronous-logic Circuit
Asynchronous-logic Circuit

FIG. 7A

700a



FIG. 7B

700b

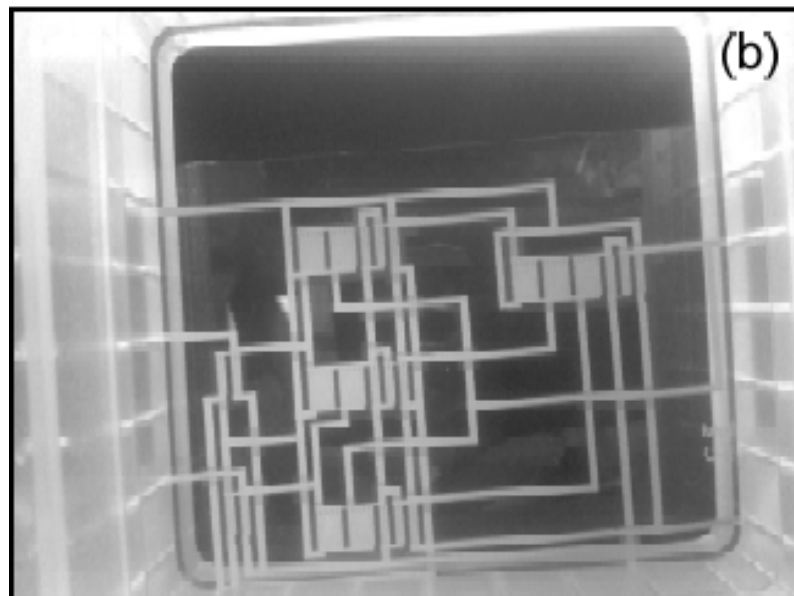


FIG. 7C

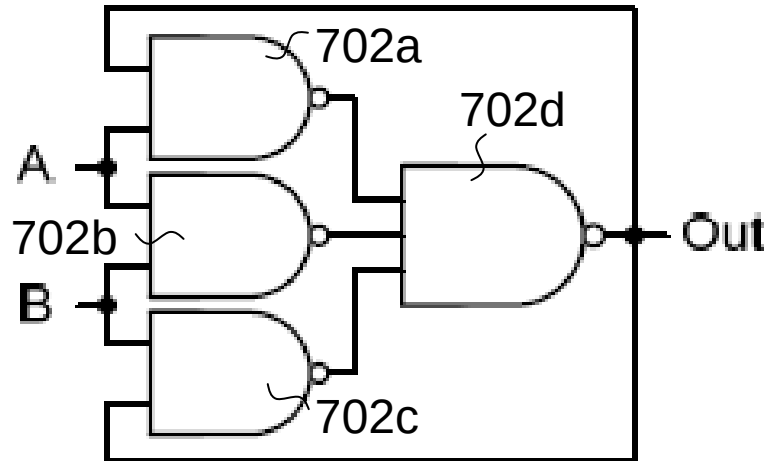
700c

FIG. 7D

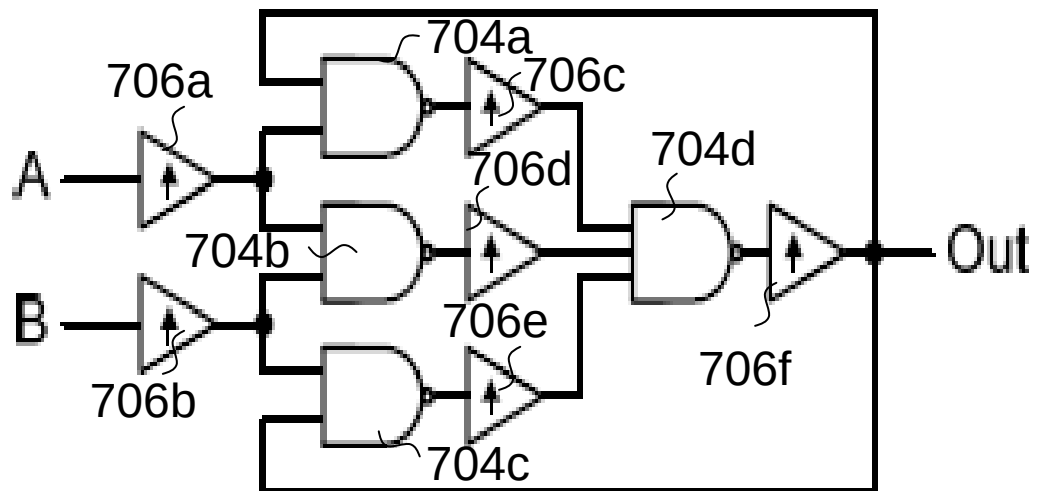
700d

FIG. 7E

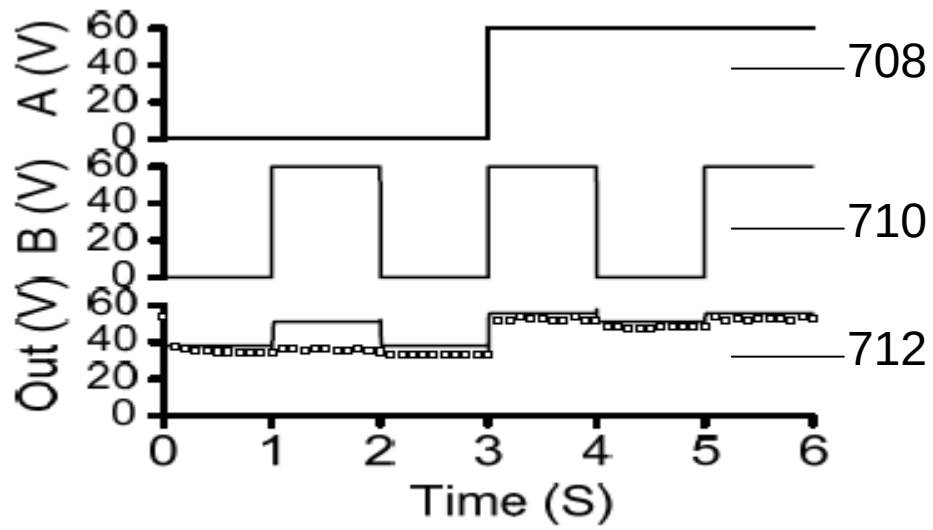
700e

FIG. 7F

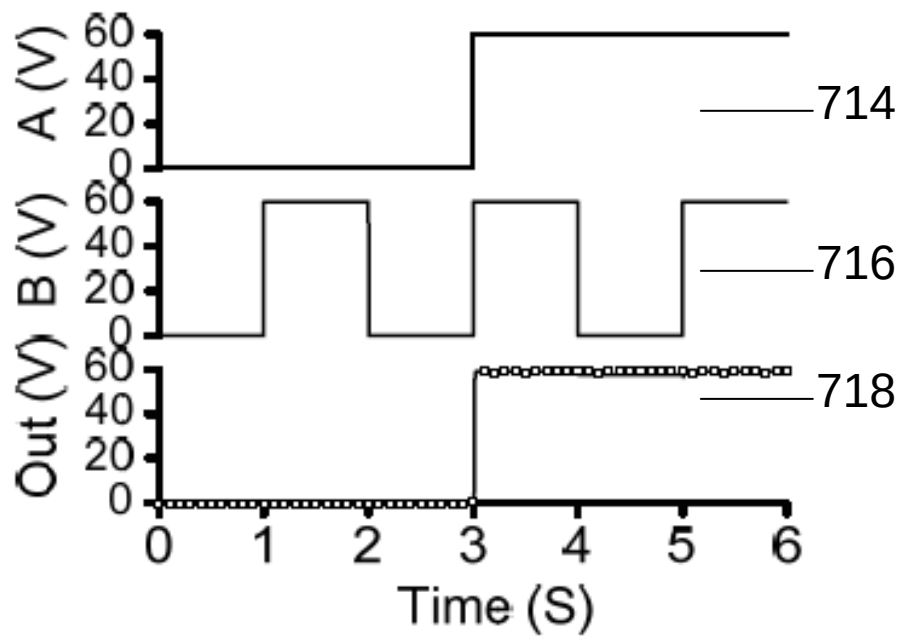
700f

FIG. 8800