Description

The present invention relates to a semiconductor trench capacitor structure that provides for high capacitance storage and allows the capacitors to abut adjacent devices. The invention also relates to a dynamic memory cell employing the trench capacitor structure, to an array of such dynamic memory cells, and to a method of producing the trench capacitor structure.

Parallel with the recent exponential growth in the use of integrated circuits, has come the development of numerous types of semiconductor memory devices. The memory device type to which the present invention pertains is a dynamic memory cell wherein a bit is represented by a charge stored in a capacitor structure. More specifically, the present invention relates to a semiconductor trench capacitor cell whose construction facilitates greater storage capacity, and the ability to construct more densely packed memory arrays.

Many different types of semiconductor trench and storage capacitor constructions have been proposed. Prior art of which Applicant is aware, includes: U.S. Patent 4,238,278 issued to Antipov 9 December 1980; IBM Technical Disclosure Bulletin, Vol. 27, No. 11, April 1985 concerning a "Dynamic RAM cell with merged drain and storage"; and IBM Technical Disclosure Bulletin, Vol. 28, No. 6, November 1985 concerning a "CMOS dynamic random access memory cell". These prior art approaches will now be described in greater detail.

In U.S. Patent 4,238,278, there is described a method for making both shallow and deep recessed oxide isolation trenches in semiconductor substrates. Antipov results in both shallow and deep recessed isolation trenches in which a thick oxide isolation layer is used along the entire wall surface of the trench.

IBM Technical Disclosure Bulletin, Vol. 27, No. 11, and IBM Technical Disclosure Bulletin, Vol. 28, No. 6 disclosure trench capacitor cells, whereby a recessed oxide (ROX) isolation layer is constructed between adjacent trench capacitor cells. This type of approach will be illustrated and described with reference to Figure 1, wherein a composite semiconductor substrate 10 is shown to have an N- well portion 30 formed in a P+ substrate 20. On the surface of the composite semiconductor substrate 10, there is constructed a transistor consisting of a P+ source diffusion 50, a gate electrode 60, and a P+ drain diffusion 70, the gate electrode 60 being separated from substrate 10 by a thin insulation layer 15. To the left of the source 50, there is shown a partial section of a recessed oxide isolation layer 99 which can be used to support and insulate additional memory array circuitry (e.g. wordlines and bitlines, not shown). Below the drain 70 there is disclosed a prior art semiconductor trench capacitor cell 40. The semiconductor trench capacitor cell 40 is constructed of a trench having a thin insulation layer 90 disposed upon its walls, the remainder of the trench being filled with a layer of doped polysilicon 80. The polysilicon material 80 is a conductive material such that it serves as a conductive electrode which is insulated from the semiconductor substrate 10 by the thin insulation layer 90. The trench capacitor cell 40 is able to store charge in the polysilicon material 80, and thus to function as a capacitor.

To the right of the semiconductor trench capacitor cell 40 in Fig. 1, there is also constructed an adjacent semiconductor trench capacitor cell 110. The adjacent semiconductor trench cell capacitor also has a thin insulation layer 130, and is filled with a polysilicon material 120. These semiconductor trench capacitor cells 40 and 110 are necessarily placed apart and are isolated from one another by the Recessed Oxide (ROX) isolation layer 100. The need for separation and isolation of the adjacent semiconductor trench capacitor cells 40 and 110 is due to electrical device limitations. If the semiconductor trench capacitor cells 40 and 110 are not provided with the necessary isolation, there would be numerous incidences of interference due to the electrical interaction between adjacent semiconductor trench capacitor cells.

Although the above described approach allows the construction of trench capacitor cells which avoid interference and breakdown problems, this construction has been found to be impracticable in the construction of densely packed memory arrays. As the number of dynamic memory cells to be fabricated on a semiconductor substrate increases above one million, there will be a limitation on the amount of substrate surface area which can be devoted to each individual memory cell.

As shown in Fig. 1, surface isolation regions such as ROX regions 99 and 100 consume an appreciable percentage of the total chip surface area. It would be beneficial to reduce the amount of chip surface area consumed by these isolation regions, while at the same time preserving the integrity of the charge stored in adjacent memory cells.

Consequently, there exists a need for an improved approach in the construction of semiconductor trench capacitor cells to facilitate construction of densely packed arrays. More specifically, there exists a need for improvements which allow both the construction of trench capacitor cells having greater storage capacity, making a more efficient use of the semiconductor substrate area.

EP-A-0 167 764, entitled "Dynamic Ram cell", published January 15, 1968 relates to a trench cell in which a polysilicon-filled trench extends through

a well region formed on an epitaxial region, into the underlying substrate.

PATENT ABSTRACTS of JAPAN, vol. 8, no. 103 (E-244)[1540], May 15, 1984 & JP-A- 59 019 366, published January 31, 1984 relates to a semiconductor trench structure in which the trench is filled with a conductive electrode and where upper portions of the side-wall isolation of the trench are thicker than lower portions.

It is an important object of this invention to provide a semiconductor trench capacitor having increased size, and therefore increased charge storage capacity.

It is a second object of this invention to provide a method of constructing a semiconductor trench capacitor which has an isolation structure within the filled trench.

It is another object of this invention to provide a semiconductor trench capacitor structure which facilities the construction of densely packed arrays.

It is still a further object of the present invention to provide a semiconductor trench capacitor structure which can be closely placed to adjacent semiconductor trench capacitor structures.

The present invention as claimed provides a unique approach to satisfy the aforementioned needs and objects. More specifically, the present invention uses an approach of merging the isolation layer and node trench such that the isolation regions are self aligned to the trench side walls. Thus, trench capacitors of higher capacity can be constructed in a given space. Moreover, these larger trench capacitors can be placed more closely to adjacent trench capacitor cells. As a result, the overall area of the semiconductor substrate is more efficiently utilized, and trench capacitor cells of sufficient charge storage capacity to facilitate the construction of densely packed memory arrays are realized.

Accordingly, the present invention relates to a semiconductor trench capacitor structure, comprising: a semiconductor substrate; a trench formed in said semiconductor substrate, said trench having a bottom wall, and a side wall which has an upper side wall portion and a lower side wall portion; a thin insulating layer formed on said bottom wall and said lower side wall portion; a thick isolating layer formed on a portion of said upper side wall portion to provide isolation; and a conductive electrode formed of a conductive material filling the remainder of said trench.

The present invention also relates to a method of producing a semiconductor trench capacitor structure having an isolation region formed within its trench, said method comprising: forming a trench in a semiconductor substrate, said trench defined by a bottom wall and a side wall having an upper side wall portion and a lower side wall portion; forming a thin insulating layer on said bottom wall and said lower side wall portion; forming a thick insulating layer on at least a portion of said upper side wall portion; and, filling the remainder of said trench with a conductive material.

One way of carrying out the invention is described in detail below with reference to drawings which illustrate a specific embodiment and in which:

Figure 1 is a diagram showing the construction of a dynamic memory cell with a prior art semiconductor trench capacitor cell.

Figure 2 is a diagram showing the construction of a dynamic memory cell with a semiconductor trench capacitor cell of the present invention.

Figures 3A through 3H show the steps used in the fabrication of a semiconductor trench capacitor cell of the present invention.

Figure 4A is a magnified top plan view of a portion of a semiconductor substrate showing an example of the size of semiconductor substrate area devoted to a memory cell capacitor, when the prior art recessed oxide isolation approach is used to construct a dynamic memory array.

Figure 4B is a cross-sectional view taken along lines A-A′ of Figure 4A.

Figure 5A is a magnified top plan view of a preferred array layout embodiment of the present invention.

Figure 5B is a cross-sectional view taken along lines B-B′ of Figure 5A.

Figure 6 is a top plan view of a portion of a semiconductor substrate showing an alternate array layout embodiment of the present invention.

Figure 7 is a top plan view of a portion of a semiconductor substrate showing another alternate array layout embodiment of the present invention.

Turning now to Figure 2, a dynamic memory cell with a semiconductor trench capacitor cell structure of the present invention is shown. The dynamic memory cell is formed in a composite semiconductor substrate 210 in which an N- well 230 is formed in a P+ substrate portion 220. On the surface of the semiconductor substrate 210, a transistor is constructed of a P+ drain diffusion 250, a gate electrode 260, and a P+ source diffusion 270. The insulation between the gate electrode 260 and the substrate as well as the thin insulating layer on top of the drain diffusion 250 and source diffusion 270 is shown schematically as a single thin insulation layer 215. To the left of the drain 250, there is shown a partial section of a Recessed Oxide layer 299 which can be used to support and insulate additional memory array circuitry (e.g. wordlines and bitlines, not shown). Adjacent to the source diffusion 270 is a semiconductor trench

capacitor cell 240 of the present invention. The semiconductor trench capacitor cell 240 is insulated from the semiconductor substrate 210 by a thin insulation layer 290, and is isolated from adjacent semiconductor trench capacitor cells by sidewall defined, thick isolation layers 340 and 350. Also shown for illustration is another semiconductor trench capacitor cell 310. The semiconductor trench capacitor cell 310 is also insulated from the semiconductor substrate 210 by a thin insulation layer 330, and is isolated from adjacent devices by thick isolation layers 380 and 390. Both semiconductor trench capacitor cells are filled with a P+ doped conductive polysilicon 280 and 320 respectively.

As can be seen by a comparison of the present invention in Figure 2 with the prior art device in Figure 1, the Recessed Oxide isolation layer 100 between adjacent semiconductor trench capacitor cells 40 and 110 in Figure 1, has been supplemented by an alternative structure. Instead of relying solely upon a Recessed Oxide isolation layer disposed on the surface of the substrate to isolate adjacent semiconductor trench capacitor cells, the isolation structure of the present invention is formed within the trench. By forming an isolation structure that is self-aligned to the trench side walls, extra chip space that was devoted to isolating the trench from the channel of the adjacent transistor device is no longer needed. In effect, since the isolation is defined by the trench side wall itself, the trench can now abut the channel of an adjacent transistor. This greatly increases the size of the trench capacitor, enhancing its charge storage capacity.

A comparison of Figs. 1 and 2 does not immediately reflect the advantages of the invention. That is, as shown in the particular cross-section of Fig. 2, (i.e. from top-to-bottom of the overhead view of the invention as shown in Fig. 5), the cell area of the invention appears to be equivalent to that realized by the prior art cell as shown in Fig. 1. However, as will be described in relation to Figs. 4 and 5, the capacitor-to-adjacent transistor device spacing is greatly decreased by utilization of the present invention.

Turning now to Figure 3A, an illustration is shown of the beginning step in constructing a semiconductor trench capacitor cell of the present invention. A semiconductor substrate 210 is shown with an N- well 230 formed in the P+ substrate 220. A thin insulation layer 215 is then formed along the surface of the semiconductor substrate 210 via known semiconductor methods, for example, via oxidation growth or chemical-vapor-deposition.

Turning now to Figure 3B, the next step of construction is shown. A masking oxide layer 550 has been formed on top of the thin insulation layer 215, and has been patterned to allow a trench 560 to be formed down into the semiconductor substrate 210. The trench 560 can be formed via known semiconductor methods, for example, reactive-ion-etching (RIE) in a chlorine gas. The trench 560 is defined by a bottom wall 655, and a side wall 650 having an upper side wall portion 660 and a lower side wall portion 670. These side walls are defined by an etch to be described below. In a preferred embodiment, the upper side wall portion 660 occupies approximately the top 10% to 20% of the side walls 650, and the lower side wall portions 670 occupies approximately the lower 80% to 90% of the side walls 650. However, it should be noted that these percentages are only exemplary of the preferred embodiment, the present invention also being useful with other upper and lower side wall arrangements.

It should also be noted that the vertical cross sections of the trench constructions in the present application have been illustrated as rectangular to simplify the description. The scope of the present invention is by no means meant to be limited to trench constructions of this geometric shape. In fact, in using practical semiconductor methods, the formation of a perfectly rectangular trench is probably impracticable; the trench is much more likely to have a vertical side wall which merges to form a round cupped bottom rather than a perpendicular flat bottom.

In the next step of construction shown in Figure 3C, a thin insulating layer 290 is formed along the trench side walls 650. This thin insulating layer 290 may be formed by known semiconductor methods, for example, oxidation growth or chemical-vapor-depositing. This insulating layer may be comprised of silicon oxide, silicon nitride, or a composite of both materials. Next in Figure 3D the trench 560 is filled with a polysilicon fill 580. The polysilicon fill 580 is doped with boron to form a P+ conductive material which will facilitate the storage of charge in the final semiconductor trench capacitor structure. Note that the polysilicon fill 580 is insulated from the semiconductor substrate 210 by the thin insulating layer 290.

After the trench 560 has been filled with the polysilicon fill 580, a portion of the polysilicon 580 is removed from the trench 560, exposing the upper portion of the trench side walls. The point at which the removal is terminated will define the top of the trench lower side wall portions 670. This is shown in Figure 3E, and in the preferred embodiment the polysilicon fill 580 would be left in the lower 80% of the trench 560. After the polysilicon fill 580 has been removed to this level, thick isolating layers 340 and 360 are formed along the trench upper side wall portions 660. These thick isolating

layers 340 and 360 are formed by chemical-vapor-deposition of a conformal isotropic isolating layer, such as silicon oxide, followed by an anisotropic etch (e.g. RIE) that removes the horizontal portions of the oxide without removing the vertical portions coated on the side walls of the trench. In a preferred embodiment, the thick isolating layers 340 and 360 would be formed along the trench upper side wall portions with a thickness of about 150 nm. Note that these thick isolating layers 340 and 360 effectively correspond to the recessed oxide isolating layer 100 in Figure 1, yet the thick isolating layers 340 and 360 represent an isolation structure formed within the trench.

After the thick isolating layers 340 and 360 are formed as shown in Figure 3E, a layer of photoresist 700 is formed along the top of the semiconductor substrate 210, including the trench 560. The resist 700 is exposed and developed to expose a portion of the thick isolating layer 360 and the thin insulating layer 290. As shown in Figure 3F, the exposed oxide layers are then removed. This removal can be conducted via known semiconductor methods, for example, reactive ion etching (RIE) in a gas. After the portion of the thick isolating layer 360 and the thin insulating layer 290 has been removed, the resist 700 is then removed. The step shown in Figure 3F is used to define a "buried contact" that couples the source diffusion region 270 to the polysilicon inside the trench. As shown in the aforementioned EP-A-0 167 764, this mask step could be eliminated by providing a separate conductor layer on top of the substrate to form a "bridge contact" that couples the source diffusion to the poly-filled trench. In the present invention, both the "buried contact" and the "bridge contact" are contemplated. The depicted buried contact embodiment is preferred. After the resist 700 has been removed, the upper portion of the trench 560 is refilled with a polysilicon refill 800. This is shown in Figure 3G.

Once the upper portion of the trench 560 has been refilled and the masking oxide layer 550 has been removed, the top surface of the polysilicon refill 800 is removed (or planarized) to a level slightly below the level which coincides with the top level of the silicon substrate 210. See Figure 3H. Once the polysilicon refill 800 has been slightly removed, a thick isolating layer 350 is formed along the top of the trench 560. In a preferred embodiment, the thick isolating layer 350 is formed to a thickness of approximately 150 nm. If the "bridge contact" embodiment is used, the conductive material would be deposited and patterned to form the bridge contact, and isolation layer 350 would be deposited on top of the bridge contact. The top surface of the thick isolation layer 350 can then be planarized to coincide with the top surface of the semiconductor substrate 210. Thus, there is formed a trench capacitor cell having an isolating structure 340, 350 and 360 within its trench.

The formation of the transistor shown in Figure 2 is not herein described, its formation being well known in the art. It should be noted that during the anneal cycle that drives in the P+ dopants to define the drain diffusion, dopant ions will diffuse from the refill polysilicon 800 into the adjacent substrate portion to define the source diffusion 270. The "buried contact" is now defined by the portions of source diffusion 270 and polysilicon refill 800 that are in contact with one another.

As an illustration of the increased capacitor size and the more efficient use of semiconductor substrate area, two additional figures are shown. Figure 4A shows a magnified top plan view of a portion of a dynamic memory array constructed on a semiconductor substrate 400 using the prior art Recessed Oxide isolation approach. In looking downward toward the top surface of the semiconductor substrate 400, there is shown the outline of the side walls of two memory cell capacitors indicated by the thin dashed lines 405 and 410. Shown running from left to right are wordlines 415 and 420. It should be noted that the wordlines are formed of a polysilicon material that defines the gate electrode 60 of the device shown in Figure 1. The wordlines 415 and 420 are separated from the top surface of the semiconductor substrate by an oxide layer. Next, shown running from top to bottom are bitlines 425 and 430. These bitlines are normally of a metal material, and are separated from the wordlines and semiconductor substrate by another oxide layer. The wordline 415 and the bitline 425 are associated with the memory cell capacitor 410, while the wordline 420 and bitline 430 are associated with the memory cell capacitor 405. Thus, adjacent memory cells are coupled in a staggered relationship with respect to both the wordlines and the bitlines. The operation of the wordlines and bitlines are not of importance with a description of the present invention, so their operation will not be described. However, the bitline and wordline illustrations are of importance in noting the device spacings which are required when the prior art Recessed Oxide approach is used as shown in Figure 4A. In particular, with the Recessed Oxide approach, there is a minimum distance d_1 which must be maintained between the memory cell capacitor 410 and the gate electrode of the adjacent memory cell as defined by wordline 420. This minimum distance must be maintained to avoid electrical interferences (i.e. leakage from the channel region of the adjacent memory cell). These minimum distance requirement leads to much wasted semiconductor substrate area as can be seen in the top plan view of Figure 4A.

The present invention realizes great improvement in the increased efficient usage of semiconductor substrate area. In Figure 5A, there is shown a magnified top plan view of a portion of a dynamic memory array constructed on a semiconductor substrate 500 using the trench isolation approach of the present invention. In a layout manner similar to that shown and described for Figure 4A, there is shown memory cell capacitors 505 and 510, wordlines 515 and 520, and bitlines 525 and 530. In Figure 5A, wordline 515 and bitline 525 are associated with the memory cell capacitor 510, while wordline 520 and bitline 530 are associated with memory cell capacitor 505. Again, the memory cells are connected in a staggered relationship with respect to both the wordlines and the bitlines. In Figure 5A, the memory cell capacitors 505 and 510 have been constructed using the trench isolation approach of the present invention. Several advantages are realized as can be easily seen in the top plan view of Figure 5A. First, the memory cell capacitor size is shown to have been increased by a factor of approximately 3 in the lateral (i.e., left-to-right) direction. The capacitor has assumed an elongated, rectangular shape as opposed to the square shape in the prior art as shown in Figure 4A. As the size of the memory cell capacitor has been increased, so has its charge storage capacity. This is due to the elimination of a ROX region in this direction, as described below.

Next, as can be seen in Figure 5A, the minimum distance d_2 required between the memory cell capacitor 510 and the gate electrode of the adjacent memory cell as defined by wordline 520 is effectively equal to zero. That is, since the isolation is self-aligned with respect to the inside edges of the capacitor, the capacitor can now abut the channel region of the adjacent device without leakage concerns. In fact, the memory cell capacitor 510 and adjacent memory cells' bit line (530) are able to be slightly overlapped. Thus, it can be seen that the trench isolation approach of the present invention results in a more efficient use of the semiconductor surface area.

The advantages of the present invention are most clearly shown by a comparison of Figure 4B and Figure 5B. Figure 4B is a cross-sectional view taken along lines A-A′ in Figure 4A. The space d_1 in Figure 4A is shown as a ROX region in Figure 4B that separates the channel region of the gate electrode from the capacitor 410. Figure 5B is a cross-sectional view taken along lines B-B′ in Figure 5A. Note that there is no ROX region corresponding to the ROX region in Figure 4B such that the capacitor 510 abuts the channel region beneath the gate electrode of the transistor of the adjacent memory cell. Also, because there is no ROX region to consume chip area, the capacitor 510 is much wider (i.e. longer in the left-to-right dimension) than is capacitor 410 as shown in Figure 4B. In practice, in the array shown in Figure 5A, both of the short sides of the rectangular-shaped capacitor 410 will abut the channel regions of adjacent memory cell transistors. Furthermore, note from Fig. 5A that the buried contact between the poly filled trench and the source diffusion of the associated FET (i.e. the portion of the trench side walls in which the side wall defined isolation layers are partially removed) is located at approximately the midpoint of the long side of the trench, far removed from the channel regions of the adjacent transistors.

As a result of the hereinbefore mentioned embodiments of the present invention, a semiconductor trench capacitor cell is furnished having its isolation structure formed within and self-aligned to the trench side walls. With the isolation structure formed within the trench, capacitor cell size can be increased, thus facilitating the construction of memory arrays which can be more density packed.

Utilizing the trench capacitor structure of the present invention, other array layout embodiments can be constructed that maximize cell area while minimizing chip space. In the layout embodiment of the invention as shown in Fig. 5A, ROX regions are still formed between adjacent trench capacitors. In the layouts shown in Figures 6 and 7, these ROX regions are eliminated. In Fig. 6, the capacitors 505, 510 are reconfigured so that they are perpendicular to the wordlines 515, 520. That is, the trench-to-trench spacing is now a function of defining a space for the source diffusion, rather than defining a ROX region as in Fig. 5A. In another layout embodiment of the present invention as shown in Fig. 7, the metal bitlines 525, 530 of Fig. 5A are replaced by diffused bitlines and a metal wordline 515B runs through the central portion of the layout. Again, there is no ROX region between adjacent capacitors.

Claims

1. A semiconductor trench capacitor structure (240), comprising:
   a semiconductor substrate (210);
   a trench (560) formed in said semiconductor substrate (210), said trench (560) having a bottom wall (655), a side wall (650) having an upper side wall portion (660) and a lower side wall portion (670);
   a thin insulating layer (290) formed on said bottom wall (655) and said lower side wall portion (670);
   a thick isolating layer (340, 360), **providing for isolation to neighboring structures,** formed on at least part of said upper side wall portion

The present invention realizes great improvement in the increased efficient usage of semiconductor substrate area. In Figure 5A, there is shown a magnified top plan view of a portion of a dynamic memory array constructed on a semiconductor substrate 500 using the trench isolation approach of the present invention. In a layout manner similar to that shown and described for Figure 4A, there is shown memory cell capacitors 505 and 510, wordlines 515 and 520, and bitlines 525 and 530. In Figure 5A, wordline 515 and bitline 525 are associated with the memory cell capacitor 510, while wordline 520 and bitline 530 are associated with memory cell capacitor 505. Again, the memory cells are connected in a staggered relationship with respect to both the wordlines and the bitlines. In Figure 5A, the memory cell capacitors 505 and 510 have been constructed using the trench isolation approach of the present invention. Several advantages are realized as can be easily seen in the top plan view of Figure 5A. First, the memory cell capacitor size is shown to have been increased by a factor of approximately 3 in the lateral (i.e., left-to-right) direction. The capacitor has assumed an elongated, rectangular shape as opposed to the square shape in the prior art as shown in Figure 4A. As the size of the memory cell capacitor has been increased, so has its charge storage capacity. This is due to the elimination of a ROX region in this direction, as described below.

Next, as can be seen in Figure 5A, the minimum distance d_2 required between the memory cell capacitor 510 and the gate electrode of the adjacent memory cell as defined by wordline 520 is effectively equal to zero. That is, since the isolation is self-aligned with respect to the inside edges of the capacitor, the capacitor can now abut the channel region of the adjacent device without leakage concerns. In fact, the memory cell capacitor 510 and adjacent memory cells' bit line (530) are able to be slightly overlapped. Thus, it can be seen that the trench isolation approach of the present invention results in a more efficient use of the semiconductor surface area.

The advantages of the present invention are most clearly shown by a comparison of Figure 4B and Figure 5B. Figure 4B is a cross-sectional view taken along lines A-A′ in Figure 4A. The space d_1 in Figure 4A is shown as a ROX region in Figure 4B that separates the channel region of the gate electrode from the capacitor 410. Figure 5B is a cross-sectional view taken along lines B-B′ in Figure 5A. Note that there is no ROX region corresponding to the ROX region in Figure 4B such that the capacitor 510 abuts the channel region beneath the gate electrode of the transistor of the adjacent memory cell. Also, because there is no ROX region to consume chip area, the capacitor 510 is much wider (i.e. longer in the left-to-right dimension) than is capacitor 410 as shown in Figure 4B. In practice, in the array shown in Figure 5A, both of the short sides of the rectangular-shaped capacitor 410 will abut the channel regions of adjacent memory cell transistors. Furthermore, note from Fig. 5A that the buried contact between the poly filled trench and the source diffusion of the associated FET (i.e. the portion of the trench side walls in which the side wall defined isolation layers are partially removed) is located at approximately the midpoint of the long side of the trench, far removed from the channel regions of the adjacent transistors.

As a result of the hereinbefore mentioned embodiments of the present invention, a semiconductor trench capacitor cell is furnished having its isolation structure formed within and self-aligned to the trench side walls. With the isolation structure formed within the trench, capacitor cell size can be increased, thus facilitating the construction of memory arrays which can be more density packed.

Utilizing the trench capacitor structure of the present invention, other array layout embodiments can be constructed that maximize cell area while minimizing chip space. In the layout embodiment of the invention as shown in Fig. 5A, ROX regions are still formed between adjacent trench capacitors. In the layouts shown in Figures 6 and 7, these ROX regions are eliminated. In Fig. 6, the capacitors 505, 510 are reconfigured so that they are perpendicular to the wordlines 515, 520. That is, the trench-to-trench spacing is now a function of defining a space for the source diffusion, rather than defining a ROX region as in Fig. 5A. In another layout embodiment of the present invention as shown in Fig. 7, the metal bitlines 525, 530 of Fig. 5A are replaced by diffused bitlines and a metal wordline 515B runs through the central portion of the layout. Again, there is no ROX region between adjacent capacitors.

Claims

1. A semiconductor trench capacitor structure (240), comprising:
   a semiconductor substrate (210);
   a trench (560) formed in said semiconductor substrate (210), said trench (560) having a bottom wall (655), a side wall (650) having an upper side wall portion (660) and a lower side wall portion (670);
   a thin insulating layer (290) formed on said bottom wall (655) and said lower side wall portion (670);
   a thick isolating layer (340, 360), **providing for isolation to neighboring structures,** formed on at least part of said upper side wall portion

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(660) **such that it extends into said trench (560), the outer part of said thick isolating layer (340, 360) being aligned to the side wall (650) of the trench (560);** and
a conductive electrode formed of a conductive material (580, 800) filling said trench (560).

2. A semiconductor trench capacitor (240) structure as claimed in claim 1, further comprising:
a second thick isolating layer (350) formed on the top of said conductive electrode.

3. A semiconductor trench capacitor structure (240) as claimed in claim 1, further comprising:
a buried contact for coupling said conductive electrode to a diffusion region (270) formed in said semiconductor substrate (210), said buried contact being formed by a part of said upper side wall portion (660) of said trench side wall (650) that does not have said thick isolating layer (340, 360) formed thereon.

4. A semiconductor trench capacitor structure as claimed in claim 1, wherein said thick isolating layer (340, 360) is at least 75 nano-meters in thickness.

5. A dynamic memory cell, comprising a transistor having source (270), gate (260) and drain (250) electrodes and an associated trench capacitor (240) formed in a semiconductor substrate (210), said capacitor comprising:
a trench (560) formed in the substrate (210), said trench (560) having a bottom wall (655) and a side wall (650);
a dielectric layer (290) formed on said bottom wall (655) and on lower portions (670) of said side wall (650);
a thick isolating layer (340, 360), providing for isolation to neighboring structures (100, 310), formed on at least an upper portion (660) of said side wall (650) **such that it extends into said trench (560), the outer part of said thick isolating layer (340, 360) being aligned to the side wall (650) of the trench (560);**
at least one layer (580, 800) of doped polysilicon filling said trench (560); and
a buried contact for coupling a portion of said doped polysilicon layer (800) abutting a part of said upper portions (660) of said side wall (650) that does not have said side wall-defined isolation layer (340, 360) formed thereon to an adjacent one (270) of the source and drain electrodes of the transistor.

6. An array of dynamic memory cells, each of said cells comprising a transistor disposed in a first direction and having source, gate, drain electrodes, and a channel region below the gate, and a trench storage capacitor (505, 510) **formed in a semiconductor substrate,** said capacitor (505, 510) being coupled to one of the source and drain electrodes of the transistor, said array comprising:
a plurality of wordlines (515, 520) disposed in a second direction orthogonal to said first direction, said wordlines interconnecting the gate electrodes of the transistors of the cells in a staggered relationship; and
a plurality of bitlines (525, 530) disposed in said first direction, said bitlines (525, 530) interconnecting one of the source and drain electrodes of the transistors of the cells in a staggered relationship;
each of the storage capacitors (505, 510) comprising
- **a trench formed in said semiconductor substrate, said trench having a bottom wall, a side wall having an upper side wall portion and a lower side wall portion;**
- **a thin insulating layer formed on said bottom wall and said lower side wall portion;**
- **a thick isolating layer formed on at least part of said upper side wall portion such that it extends into said trench, the outer part of said thick isolating layer being aligned to the side wall of the trench; and**
- **a conductive electrode formed of a conductive material filling said trench;**

said thick isolation layer being situated such that it provides for an isolation to the abutted channel region of an adjacent memory cell.

7. An array of dynamic memory cells as claimed in claim 6, wherein each of the storage capacitors (505, 510) has an elongated rectangular shape.

8. An array of dynamic memory cells as claimed in claim 6, wherein each of the storage capacitors (505, 510) has two long sides and two short sides, each of said short sides of each of the storage capacitors abutting the channel region of the transistors of respective adjacent ones of the memory cells.

9. An array of dynamic memory cells as claimed in claim 8, wherein each of the storage capacitors is coupled to one of the source and drain electrodes through a selected portion of its

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side wall that does not have said thick isolation layer disposed thereon, said selected portion being located at approximately a midpoint of one of said long side of said storage capacitor walls.

Patentansprüche

1. Eine Halbleitergrabenkondensatorstruktur (240), enthaltend:
Ein Halbleitersubstrat (210);
einen in diesem Halbleitersubstrat (210) ausgebildeten Graben (560), wobei der Graben (560) eine Bodenfläche (655), eine Seitenwand (650) mit einem oberen Seitenwandteil (660) und einem unteren Seitenwandteil (670) aufweist;
eine dünne Isolierschicht (290), die auf dieser Bodenfläche (655) und dem unteren Wandteil (670) ausgebildet ist;
eine dicke Isolierschicht (340, 360), die die Isolierung gegen die benachbarten Strukturen besorgt und die auf wenigstens einem Teil dieses oberen Seitenwandteils (660) ausgebildet ist, so daß sie sich in den Graben (560), den äußeren Teil der dicken Isolierschicht (340, 360) erstreckt und gemäß der Seitenwand (650) des Grabens (560) ausgerichtet ist; und
eine leitende Elektrode, die aus leitendem Material (580, 800) besteht, das den Graben (560) ausfüllt.

2. Eine Halbleitergrabenkondensatorstruktur (240) gemäß Anspruch 1, ferner enthaltend:
eine zweite dicke Isolierschicht (350), die auf der leitenden Elektrode ausgebildet ist.

3. Eine Halbleitergrabenkondensatorstruktur (240) gemäß Anspruch 1, ferner enthaltend:
einen vergrabenen Kontakt zum Ankoppeln der leitenden Elektrode an einen im Halbleitersubstrat (210) ausgebildeten diffundierten Bereich (270), wobei dieser vergrabene Kontakt durch einen Teil des oberen Seitenwandteils (660) der Grabenseitenwand (650) gebildet wird, auf dem keine dicke Isolierschicht (340, 360) ausgebildet ist.

4. Eine Halbleitergrabenkondensatorstruktur (240) gemäß Anspruch 1, in der diese dicke Isolierschicht (340, 360) mindestens 75 nm dick ist.

5. Eine dynamische Speicherzelle, enthaltend einen Transistor mit einer Source- (270), einer Gate- (260) und einer Drain-Elektrode (250) und einem zugeordneten Grabenkondensator (240), der in einem Halbleitersubstrat (210) ausgebildet ist, wobei dieser Kondensator enthält:
Einen Graben (560), der im Substrat (210) ausgebildet ist, wobei dieser Graben (560) eine Bodenfläche (655) und eine Seitenwand (650) aufweist;
eine dielektrische Schicht (290), die auf dieser Bodenfläche (655) und an unteren Teilen (670) der Seitenwand (650) ausgebildet ist;
eine dicke Isolierschicht (340, 360), die die Isolierung gegen benachbarte Strukturen (100, 310) besorgt und die mindestens an oberen Teilen (660) der Seitenwand (650) ausgebildet ist, so daß sie sich in den Graben (560) erstreckt, wobei der äußere Teil dieser dicken Isolierschicht (340, 360) nach der Seitenwand (650) des Grabens (560) ausgerichtet ist;
mindestens eine Schicht (580, 800) dotierten Polysiliziums, die diesen Graben (560) füllt; und
ein vergrabener Kontakt zum Ankoppeln eines Teils dieser dotierten Polysiliziumschicht (800), die an einem Teil der oberen Teile (660) der Seitenwand (650) anliegt, auf der keine seitenwanddefinierte Isolierschicht (340, 360) zu einer benachbarten (270) Source- oder Drain-Elektrode des Transistors ausgebildet ist.

6. Eine Anordnung dynamischer Speicherzellen, wobei jede Zelle eine Transistor enthält, der in einer ersten Richtung angeordnet ist und Source-, Gate- und Drain-Elektroden sowie einen Kanalbereich unter dem Gate, und ferner einen Grabenspeicherkondensator (505, 510), der in einem Halbleitersubstrat ausgebildet ist, aufweist, wobei dieser Kondensator (505, 510) an eine der Source- oder Drain-Elektroden des Transistors gekoppelt ist, wobei diese Anordnung enthält:
Eine Vielzahl von Wortleitungen (515, 520), die in einer zweiten Richtung senkrecht zu dieser ersten Richtung angeordnet sind und die Wortleitungen die Gate-Elektroden der Transistoren der Zellen in gegenseitig versetzter Staffelung verbindet; und
eine Vielzahl von Bitleitungen (525, 530) in dieser ersten Richtung angeordnet sind, wobei diese Bitleitungen (525, 530) eine der Source- und Drain-Elektroden der Transistoren der Zellen in versetzter Staffelung verbinden;
wobei jeder der Speicherkondensatoren (505, 510) umfaßt:
- einen Graben, der im Halbleitersubstrat ausgebildet ist und dieser Graben eine Bodenfläche, eine Seitenwand mit einem oberen Seitenwandteil und einem unteren Seitenwandteil aufweist;
- eine dünne Isolierschicht auf dieser Bodenfläche und auf dem unteren Seiten-

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wandteil ausgebildet ist;
- eine dicke Isolierschicht auf wenigstens einem Teil dieses oberen Seitenwandteils ausgebildet ist, so daß sie sich in den Graben erstreckt, wobei der äußere Teil der dicken Isolierschicht nach der Seitenwand des Grabens ausgerichtet ist; und
- eine leitende Elektrode aus einem leitenden Material ausgebildet ist, das diesen Graben füllt;

wobei die dicke Isolierschicht so angeordnet ist, daß sie die Isolierung gegen den anliegenden Kanalbereich einer benachbarten Speicherzelle liefert.

7. Eine Anordnung dynamischer Speicherzellen gemäß Anspruch 6, in der jeder Speicherkondensator (505, 510) eine längliche, rechteckige Form aufweist.

8. Eine Anordnung dynamischer Speicherzellen gemäß Anspruch 6, in der jeder Speicherkondensator (505, 510) zwei lange und zwei kurze Seiten aufweist, wobei jede kurze Seite jedes Speicherkondensators an den Kanalbereich des Transistors der jeweils benachbarten Transistoren der Speicherzellen anstößt.

9. Eine Anordnung dynamischer Speicherzellen gemäß Anspruch 8, in der jeder Speicherkondensator an eine der Source- bzw. Drain-Elektroden über einen ausgewählten Teil der Seitenwand gekoppelt ist, auf der keine dicke Isolierschicht abgelagert ist, wobei dieser ausgewählte Teil etwa in der Mitte einer der langen Seiten der Speicherkondensatorwände gelegen ist.

Revendications

1. Structure semi-conductrice (240) de condensateur à tranchée, comprenant :
un substrat semi-conducteur (210) ;
une tranchée (560) aménagée dans ledit substrat semi-conducteur (210), ladite tranchée (560) ayant une paroi inférieure (655), une paroi latérale (650) présentant une partie de paroi latérale supérieure (660) et une partie de paroi latérale inférieure (670) ;
une fine couche isolante (290) réalisée sur ladite paroi inférieure (655) et ladite partie de paroi latérale basse (670) ;
une couche isolante épaisse (340, 360), **formant isolant par rapport aux structures voisines,** aménagée sur au moins une partie de ladite partie de paroi latérale supérieure (660) **de façon à s'étendre jusque dans ladite tranchée (560), la partie externe de ladite couche isolante épaisse (340, 360) étant alignée avec la paroi latérale (650) de la tranchée (560) ;** et
une électrode conductrice composée d'un matériau conducteur (580, 800) remplissant ladite tranchée (560).

2. Structure semi-conductrice (240) de condensateur à tranchée selon la revendication 1, comportant en outre:
une seconde couche isolante épaisse (350) aménagée sur le dessus de ladite électrode conductrice.

3. Structure semi-conductrice (240) de condensateur à tranchée selon la revendication 1, comprenant en outre :
un contact enterré pour le couplage de ladite électrode conductrice à une région de diffusion (270) aménagée dans ledit substrat semi-conducteur (210), ledit contact enterré étant formé par une portion de ladite partie de paroi latérale supérieure (660) de ladite paroi latérale de tranchée (650) dénuée de couche isolante épaisse (340, 360).

4. Structure semi-conductrice (240) de condensateur à tranchée selon la revendication 1, dans laquelle ladite couche isolante épaisse (340, 360) possède une épaisseur d'au moins 75 nano-mètres.

5. Une cellule de mémoire dynamique comportant un transistor pourvu d'électrodes de source (270), de grille (260) et de drain (250) et un condensateur à tranchée (240) associé aménagé sur un substrat semi-conducteur (210), ledit condensateur comprenant :
une tranchée (560) réalisée dans le substrat (210), ladite tranchée (560) ayant une paroi inférieure (655) et une paroi latérale (650) ;
une couche diélectrique (290) aménagée sur **ladite paroi inférieure (655)** et sur les parties inférieures (670) de ladite paroi latérale (650) ;
une couche isolante épaisse (340, 360) formant isolant par rapport aux structures voisines (100, 310), réalisée sur au moins une partie supérieure (660) de ladite paroi latérale (650) **de sorte à s'étendre à l'intérieur de ladite tranchée (560), la partie externe de ladite couche épaisse isolante (340, 360) étant alignée par rapport à la paroi latérale (650) de la tranchée (560) ;**
au moins une couche (580, 800) de polysilicium dopé remplissant ladite tranchée (560) ; et
un contact enterré pour le couplage d'une por-

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tion de ladite couche de polysilicium dopé (800) aboutant une partie desdites parties supérieures (660) de ladite paroi latérale (650) qui ne comporte pas ladite couche d'isolation (340, 360) définie par la paroi latérale jusqu'à une couche adjacente (270) des électrodes de source et de drain du transistor.

6. Un réseau de cellules de mémoire dynamique, chacune desdites cellules comprenant un transistor disposé selon une première direction et pourvu d'électrodes de source, de grille, et de drain, et une région canal sous la grille, ainsi qu'un condensateur de stockage (505, 510) à tranchée **réalisé sur un substrat semi-conducteur,** ledit condensateur (505, 510) étant couplé à l'une des électrodes de source ou de drain du transistor, ledit réseau comprenant :
une pluralité de lignes de mots (515, 520) disposées dans une seconde direction orthogonale à ladite première direction, lesdites lignes de mots interconnectant les électrodes de grille des transistors des cellules selon un motif décalé ; et
une pluralité de lignes d'éléments binaires (525, 530) disposées selon ladite première direction, lesdites lignes d'éléments binaires (525, 530) interconnectant l'une des électrodes de source et de drain des transistors des cellules selon un motif décalé ;
chacun des condensateurs de stockage (505, 510) **comprenant:**
   - **une tranchée aménagée dans ledit substrat semi-conducteur, ladite tranchée comportant une paroi inférieure, une paroi latérale pourvue d'une partie supérieure et d'une partie inférieure ;**
   - **une fine couche isolante aménagée sur ladite paroi inférieure et sur ladite partie inférieure de paroi latérale ;**
   - **une couche isolante épaisse aménagée sur au moins une portion de ladite partie supérieure de paroi latérale de façon à s'étendre dans ladite tranchée, la partie externe de ladite couche isolante épaisse étant alignée avec la paroi latérale de la tranchée ; et**
   - **une électrode conductrice réalisée dans un matériau conducteur remplissant ladite tranchée ; ladite couche d'isolation épaisse étant située de sorte à former un isolant par rapport à la région de canal voisine d'une cellule mémoire adjacente.**

7. Un réseau de cellules de mémoire dynamique selon la revendication 6, dans lequel chacun des condensateurs de stockage (505, 510) possède une forme rectangulaire allongée.

8. Un réseau de cellules de mémoire dynamique selon la revendication 6, dans lequel chacun des condensateurs de stockage (505, 510) possède deux côtés longs et deux côtés courts, chacun desdits côtés courts de chacun des condensateurs de stockage aboutant la région canal des transistors des cellules mémoire adjacentes respectives.

9. Un réseau de cellules de mémoire dynamique selon la revendication 8, dans lequel chacun des condensateurs de stockage est couplé à l'une des électrodes de drain ou de source à travers une partie déterminée de sa paroi latérale qui ne comporte pas ladite couche isolante épaisse, ladite partie déterminée étant située approximativement à mi-chemin de l'un desdits côtés longs desdites parois de condensateur de stockage.

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