



(51) International Patent Classification:
H01L 21/00 (2006.01)

(21) International Application Number:
PCT/US2013/021345

(22) International Filing Date:
13 January 2013 (13.01.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/586,387 13 January 2012 (13.01.2012) US
61/589,224 20 January 2012 (20.01.2012) US

(71) Applicant (for all designated States except US): **TELA INNOVATIONS, INC.** [US/US]; 485 Alberto Way, Suite 115, Los Gatos, CA 95032 (US).

(72) Inventors; and

(71) Applicants (for US only): **BECKER, Scott, T.** [US/US]; 485 Alberto Way, Suite 115, Los Gatos, CA 95032 (US).
SMAYLING, Michael, C. [US/US]; 485 Alberto Way,

Suite 115, Los Gatos, CA 95032 (US). **GANDHI, Dhru-mil** [US/US]; 485 Alberto Way, Suite 115, Los Gatos, CA 95032 (US). **MALI, Jim** [US/US]; 485 Alberto Way, Suite 115, Los Gatos, CA 95032 (US). **LAMBERT, Carole** [CA/US]; 485 Alberto Way, Suite 115, Los Gatos, CA 95032 (US). **QUANDT, Jonathan, R.** [US/US]; 485 Alberto Way, Suite 115, Los Gatos, CA 95032 (US). **FOX, Daryl** [CA/US]; 485 Alberto Way, Suite 115, Los Gatos, CA 95032 (US).

(74) Agent: **WRIGHT, Kenneth, D.**; 710 Lakeway Drive, Suite 200, Sunnyvale, CA 94085 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ,

[Continued on next page]

(54) Title: CIRCUITS WITH LINEAR FINFET STRUCTURES

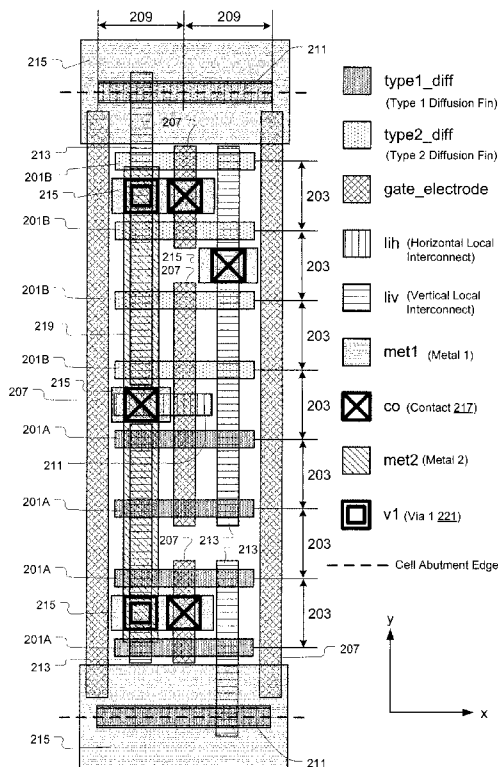


Fig. 2A

(57) Abstract: A first transistor has source and drain regions within a first diffusion fin. The first diffusion fin projects from a surface of a substrate. The first diffusion fin extends lengthwise in a first direction from a first end to a second end of the first diffusion fin. A second transistor has source and drain regions within a second diffusion fin. The second diffusion fin projects from the surface of the substrate. The second diffusion fin extends lengthwise in the first direction from a first end to a second end of the second diffusion fin. The second diffusion fin is positioned next to and spaced apart from the first diffusion fin. Either the first end or the second end of the second diffusion fin is positioned in the first direction between the first end and the second end of the first diffusion fin.



TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,

EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))