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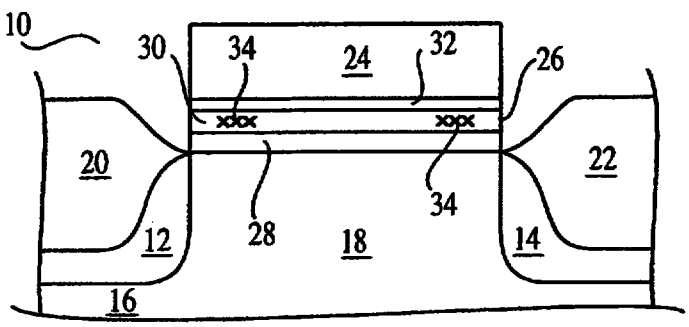
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(54) Title: HIGH TEMPERATURE OXIDE DEPOSITION FOR EEPROM DEVICES



(57) Abstract: A process for fabricating an ONO floating-gate electrode (26) in a two-bit EEPROM device (10) includes the formation of a top oxide layer (32) using a high-temperature-oxide (HTO) deposition process in which the HTO process is carried out at a temperature of about 700 to about 800 °C by either an LPCVD or RTCVD deposition processor. The process further includes the sequential formation of a silicon nitride layer (30) and a top oxide layer (32) using an in-situ LPCVD or RTCVD deposition process in which the silicon nitride layer (30) is not exposed to ambient atmosphere prior to the formation of the top oxide layer (32). The formation of the top oxide layer (32) using an HTO deposition process provides an improved two-bit EEPROM memory device (10) by reducing charge leakage in the ONO floating-gate electrode (26).

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