# PACKAGE-IN-PACKAGE USING THROUGH-HOLE VIA DIE ON SAW STREETS

## Field of the Invention

The present invention relates in general to semiconductor devices and, more particularly, to a through-hole via (THV) stackable semiconductor device.

## Background of the Invention

In a growing trend, semiconductor manufacturers have increasingly adopted three-dimensional (3D) interconnects and packaging for semiconductor devices. Three-dimensional interconnects give advantages such as size reduction, reduced interconnect length and integration of devices with different functionality within a respective package.

One of the various ways of implementing 3D interconnects involves the use of THV technology. THVs can be located either within a semiconductor device, or die, or outside the die along a saw street guide.

However, current THV technology poses several limitations. A via located within a semiconductor device restricts the freedom of having additional circuitry within the

semiconductor device. As can be appreciated, a respective location of a THV forecloses the placement of circuitry at that location. As a result, the functionality of the semiconductor device, and therefore, a device making use of the semiconductor device, is limited.

A via located outside the semiconductor device, i.e., along the saw street guide, necessitates a wider saw street to accommodate the creation of a through-hole. As a result, yields for semiconductor devices per wafer are reduced.

## Summary of the Invention

In light of the foregoing, the aim of the present invention is to provide a THV stackable semiconductor device without having any of the accompanying limitations previously described.

Accordingly, in one embodiment, the present invention is a semiconductor device comprising a first semiconductor die and insulating material disposed around a peripheral region of the first semiconductor die. A conductive via is formed through the insulating material. A redistribution layer including a first bond pad is formed over a surface of the first semiconductor die. A second semiconductor die is disposed over the first semiconductor die and redistribution layer.

In another embodiment, the present invention is a semiconductor device comprising a first semiconductor die and insulating material disposed around a peripheral region of the first semiconductor die. A conductive via is formed through the insulating material. A first bond pad is formed over a surface of the first semiconductor die. A conductive trace is

formed over the surface of the first semiconductor die between the conductive via and the first bond pad. A redistribution layer including a second bond pad is formed over the surface of the first semiconductor die.

In another embodiment, the present invention is a semiconductor device a first semiconductor die and insulating material disposed around a peripheral region of the first semiconductor die. A conductive via is formed through the insulating material. A redistribution layer is formed over a surface of the first semiconductor die.

In another embodiment, the present invention is a semiconductor device comprising a first semiconductor die and insulating material disposed around a peripheral region of the first semiconductor die. A conductive via is formed through the insulating material. A conductive trace is formed over a surface of the first semiconductor die and electrically coupled to the conductive via.

## Brief Description of the Drawings

FIG. 1 illustrates an exemplary prior art method of making a wafer level chip scale package;

FIGs. 2A and 2B illustrate a first embodiment of a THV stackable semiconductor device in a top and side view, respectively;

FIGs. 3A and 3B illustrate a first step in a first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 4A and 4B illustrate a second step in a first exemplary method of manufacturing the THV stackable

semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 5A and 5B illustrate a third step in a first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 6A and 6B illustrate a fourth step in a first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 7A and 7B illustrate a fifth step in a first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 8A and 8B illustrate a sixth step in a first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 9A and 9B illustrate a seventh step in a first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 10A and 10B illustrate an eighth step in a first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 11A and 11B illustrate a second embodiment of a THV stackable semiconductor device incorporating a plurality of complete THVs, as shown in a top and side view, respectively;

FIGs. 12A and 12B illustrate a third step in a second exemplary method of manufacturing the THV stackable

semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 13A and 13B illustrate a fourth step in a second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 14A and 14B illustrate a fifth step in a second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 15A and 15B illustrate a sixth step in a second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 16A and 16B illustrate a seventh step in a second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 17A and 17B illustrate an eighth step in a second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 18A and 18B illustrate a ninth step in a second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIGs. 19A and 19B illustrate a tenth step in a second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively;

FIG. 20 illustrates a third exemplary embodiment of a

THV stackable semiconductor device, shown utilizing a die-to-die stacking configuration in a side view;

FIG. 21 illustrates a fourth exemplary embodiment of a THV stackable semiconductor device, shown utilizing a die-to-die stacking configuration which incorporates solder paste, again in a side view;

FIG. 22 illustrates a fifth exemplary embodiment of a THV stackable semiconductor device, having multiple rows of bond pads and multiple rows of via holes as shown in a top view;

FIG. 23 illustrates a sixth exemplary embodiment of a THV stackable semiconductor device, incorporating a row of half-cut via holes coupled to a row of bond pads on opposing sides of a die as shown in a top view;

FIG. 24 illustrates a seventh exemplary embodiment of a THV stackable semiconductor device, incorporating dummy via holes on opposing sides as shown in a top view;

FIG. 25 illustrates an eighth exemplary embodiment of a THV stackable semiconductor device, incorporating dummy via holes on a single side as shown in a top view; and

FIG. 26 illustrates a ninth exemplary embodiment of a THV stackable semiconductor device, depicting two stacked dies utilizing the dummy via holes as shown in FIGs. 24 and 25 to connect a top die with a wire-bonding process;

FIG. 27A illustrates a die incorporating a THV die where a series of RDL and interconnection pads are disposed over the die;

FIG. 27B illustrates the series of redistribution layers and interconnection pads connecting the THV die to a second die;

FIG. 28 illustrates a wire bond die disposed over a

THV die, where the wire bond die is wire-bonded to the THV of the die;

FIG. 29 illustrates a wire bond die disposed over a THV die where the wire bond die is wire-bonded to a bond pad on the THV die;

FIG. 30 illustrates a wire bond die disposed over a THV die where the wire bond die is wire-bonded to the THV of the die and a circuit carrier substrate;

FIG. 31 illustrates a overhanging wire bond die disposed over a THV die;

FIG. 32 illustrates a flip chip die disposed over a THV die;

FIG. 33 illustrates a third die disposed over a flip chip die, where the flip chip die is coupled to the THV die;

FIG. 34 illustrates a leadframe package disposed over a THV die;

FIG. 35 illustrates an array package disposed over a THV die;

FIG. 36 illustrates an inverted package disposed over a THV die;

FIG. 37 illustrates an inverted package disposed over a THV die, where a third die is disposed over the integrated package;

FIG. 38 illustrates a THV die disposed over an inverted package;

FIG. 39 illustrates a THV die disposed over an inverted package, where a third die is disposed over the THV die;

FIG. 40 illustrates a multi-THV die configuration disposed over an inverted package;

FIG. 41 illustrates a multi-THV die configuration

disposed over an inverted package, where an additional die is disposed over a THV die;

FIG. 42 illustrates a THV die incorporating an under-hang passive device; and

FIG. 43 illustrates a THV die incorporating an over-hang passive device.

## Detailed Description of the Drawings

The present invention is described in one or more embodiments in the following description with reference to the Figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

In the following description and claims, the terms "comprise" and "include," along with their derivatives, may be used and are intended as synonyms for each other. In addition, in the following description and claims, the terms "coupled" and "connected," along with their derivatives, may be used. "Connected" may be used to indicate that two or more elements are in direct physical or electrical contact with each other. "Coupled" may mean that two or more elements are in direct physical or electrical contact. However, "coupled" may also mean that two or more elements are not in direct contact with each other, but yet still co-operate or interact with each other. For example, "coupled" may mean that two or more

elements do not contact each other but are indirectly joined together via another element or intermediate elements. Finally, the terms "on," "overlying," and "over" may be used in the following description and claims. "On," "overlying," and "over" may be used to indicate that two or more elements are in direct physical contact with each other. However, "over" may also mean that two or more elements are not in direct contact with each other. For example, "over" may mean that one element is above another element but not contact each other and may have another element or elements in between the two elements.

FIG. 1 illustrates an exemplary prior art method 100 of making a wafer level chip scale package. A plurality of semiconductor devices 102 are cut from a wafer. Each semiconductor device 102 has a plurality of protruding bonding pads 104 located on the active surface of the device.

The plurality of semiconductor devices 102 are disposed on the top surface of a retractable film 106. The retractable film 106 is secured by a frame 108. The frame 108 is fixed by a fixture 110 and retractable film 106 is displaced on a work platform 112 and then stretched.

The platform 112 can move up relative to fixture 110. The wafer is cut by a cutter into the plurality of semiconductor devices 102 as shown, which have been encapsulated into semiconductor packages, and then sawn by cutter 118. A shaft 114 moves upward to lift platform 112 relative to fixture 110.

The present invention improves upon the exemplary prior art method 100 of manufacture to render a through-hole via (THV) semiconductor device which is, in some embodiments, stacked together for specific applications and implementations.

FIGs. 2A and 2B illustrate a first embodiment of a

THV stackable semiconductor device 200, in a top and side view, respectively. Device 200 has an incorporated die 202. Device 200 includes a plurality of bond pads 204 which are deposited on an active side of semiconductor die 202. Bonding pads 204 can be deposited on the electrode terminals of die 202 by a plating process, or otherwise. The materials of bonding pads 204 can be made from a conductive metal, such aluminum (Al). Bonding pads 204 can be joined to a substrate by a soldering process.

A series of metal traces 206 electrically couple bond pads 204 to via 226. As shown in FIG. 2B, via 226 extends vertically from the active, top surface 212 of die 202 and surrounding material 210 to a bottom surface of the die and surrounding material 210, which is consistent with a THV design.

The surrounding material 210, which is, for purposes of the present invention, referred to as an “organic material”, is deposited around peripheral surface 214 of die 202 as shown. The organic material 210 is an improvement and a departure from that of the prior art, as will be further described. The organic material can include such materials as benzocyclobutene (BCB), a polyimide (PI) material, or similar material. As shown, vias 226 are formed in organic material 210 and organized according to rows. In the present embodiment 200, vias 226 are formed in each side of organic material 210, e.g., sides 216, and 218, so as to completely surround the periphery of die 202. Each of the plurality of bond pads 204 is electrically coupled to each of the plurality of vias 226.

As will be shown, THV 226 can be formed in various configurations, for example, along multiple rows. Further, half-cut vias as shown in the instant figure or complete, uncut

vias can be formed in various embodiments to suit particular implementations. The semiconductor device 200 can be stacked or coupled with additional dies 202 in a variety of configurations.

FIGs. 3A and 3B illustrate a first step in a first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively. A series of bond pads 204 are formed on an active surface of wafer 300 as shown. The wafer is designated with a saw street guide 302.

FIGs. 4A and 4B illustrate a second step in the first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively. Wafer 300 is singulated into depicted pieces 400 by a cutting source 402. Cutting source 402 can include a saw or laser cutting tool.

Prior to singulation, wafer 300 is placed on a dicing tape 404, which keeps the various segments 400 in place during the singulation process. Subsequent to the singulation process, a series of gaps 406 is formed between respective segments 400 as shown.

FIGs. 5A and 5B illustrate a third step in the first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively. Wafer 300, in the depicted respective segments, undergoes an expansion process. The dicing tape 404 can be stretched by using an expansion table to render a series of gaps 502 having predetermined distances 504. The depicted arrows 506 indicate the various expansion directions undergone by the wafer expansion process.

As a next step, FIGs. 6A and 6B illustrate a fourth

step in the first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively. The various gaps 502 shown in FIGs. 5A and 5B are filled with the previously described organic material 602. A plane 604 corresponding to a top surface of filled segments 600 is substantially coplanar with a plane 606 corresponding to a top surface of organic material 602.

The organic material 602 application can be performed by such methods as spin-coating, needle dispensing, or similar application.

FIGs. 7A and 7B illustrate a fifth step in the first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively. Segments 700 undergo a process to form a plurality of via holes 702 in organic material 602 as shown. The via holes can be formed in various processes, including a laser via drilling process or an etching process. As is shown, each of the via holes is configured in organic material 602 to correspond to respective bump pad 204 to which the via hole will be associated.

Turning to FIGs. 8A and 8B, a sixth step in the first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively, is shown. FIGs. 8A and 8B illustrate a metal patterning process, which connects a series of metal traces 206 from bond pads 204 to via holes 702. Metal traces 206 electrically connect the bond pads to each of via holes 702 locations as shown.

FIGs. 9A and 9B illustrate a seventh step in the first exemplary method of manufacturing the THV stackable

semiconductor device as shown in FIGs. 2A and 2B. A via hole metal deposition process is performed to assembly 900 to deposit conductive material into each of via holes 702, forming a series of metal vias 902. The conductive material can be materials such as Al, copper (Cu), tungsten (W), combination of metal alloys, or any other conductive metal. Again, metal vias 902 are formed in organic material 602. A variety of methods and techniques can be used to form the metal vias, such as a plating or plugging process.

FIGs. 10A and 10B illustrate an eighth step in the first exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B. Wafer assembly 300, and 900 is singulated for a second time by a cutting tool 402 to form gaps 904. The various dies 202 shown in FIGs. 10A, 10B, and the preceding exemplary figures represent a smaller portion of a totality of semiconductor devices, which are yielded from a particular wafer 300. As such, following the conclusion of the second singulation step, a majority of dies 202 are rendered to be like the embodiment shown in FIGs. 2A and 2B, where organic material 210 completely surrounds the peripheral surface of die 202, and THVs 902 are configured in rows along each side surface of the die as previously represented.

In one embodiment, following the singulation step depicted in FIGs. 10A and 10B, individual dies 202 are removed by a die pick and place process to remove each die 202 from dicing tape 404.

FIGs. 11A and 11B illustrate a second embodiment of a THV stackable semiconductor device 906 incorporating a plurality of complete THVs, as shown in a top and side view, respectively. The various features shown in the previous

figures are shown, including die 202, bond pads 204, and metal tracings, which are formed on the active surface 212 of die 202. In the instant embodiment 906, the respective THVs 908 are complete, in lieu of being half-cut as shown in the previous embodiment. The depicted complete THVs 908 can be formed by a particular configuration of saw street guide 302 as shown in FIGs. 3A and 3B. A wider saw street guide 302 allows organic material 602 to be cut as shown, retaining a complete via hole 908.

FIGs. 12A and 12B illustrate a third step in a second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively. The second method of manufacture as described shares the first two steps, i.e., providing a wafer and singulation into respective segments upon dicing tape 404, as the first exemplary method previously described. In addition, various features such as bond pads 204 are again shown.

As a next step, wafer segments 550 are picked from dicing tape 404 and placed onto a wafer support system 405 as shown. The wafer support system can logically include a second dicing tape 405. However, the wafer support system can also be a temporary wafer support system, such as glass, ceramic, laminate, or silicon (Si) substrate. In one embodiment, sawn dies 202 are picked from dicing tape 404 and placed onto wafer support system 405 using pick and place machines. The pick and place process renders a gap 406 having a predetermined width or distance 412 between respective segments 550.

FIGs. 13A and 13B illustrate a fourth step in the second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B. The organic

material 602 is again applied to segments 650 in a similar spin-coating, needle dispensing, or other manner as previously described. Plane 642 of segments 650 is substantially coplanar with plane 654 of organic material 602.

Turning to FIGs. 14A and 14B, a fifth step in the second exemplary method of manufacturing the THV stackable semiconductor device is shown in FIGs. 2A and 2B. The recoated wafer 300 is transferred onto a second wafer support system 408. The second wafer support system can again include glass, Si substrate materials, ceramic, and laminate materials.

FIGs. 15A and 15B illustrate a sixth step in the second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively. In a step 750, similar to that shown in FIGs. 7A and 7B, a plurality of via holes 702 is formed in organic material 602 to coincide with bond pads 204.

FIGs. 16A and 16B illustrate a seventh step 850 in the second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B in a side and top view, respectively. Step 850 is again similar to that shown in FIGs. 8A and 8B of metal patterning of metal traces 206 to electrically couple bond pad 204 locations to via 702 locations.

FIGs. 17A and 17B illustrate an eighth step 950 in the second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B. Vias 702 are plugged, plated or otherwise deposited with a conductive material to fill via holes 702 and render metal vias 902 as shown.

Following the metal via 902 formation process, via hole wafer 960 is transferred onto an additional dicing tape

410 as shown in FIGs, 18A and 18B, which illustrates the depicted ninth step.

FIGs. 19A and 19B illustrate a tenth step in the second exemplary method of manufacturing the THV stackable semiconductor device as shown in FIGs. 2A and 2B. A cutting tool 402 is again used to singulate via hole wafer 960 into the depicted segments 970, resulting in gaps 904. As a final step, following the second singulation process, a die pick and place machine can be utilized to again remove each device 200 from dicing tape 410.

FIG. 20 illustrates a third exemplary embodiment of THV stackable semiconductor devices 910, shown utilizing a die-to-die stacking configuration in a side view. A series of devices 200 can be stacked as shown to suit a particular application. Each of the metal vias 902 can be joined together as shown by union 912 using a direct via metal bonding process. Any number of devices 200 can be stacked as shown to realize a desired implementation.

FIG. 21 illustrates a fourth exemplary embodiment of THV stackable semiconductor devices, shown utilizing a die-to-die stacking configuration which incorporates solder paste 916, again in a side view. Solder paste 916 includes a mix of small solder particles and flux. A variety of solder pastes of various materials can be incorporated. Solder paste 916 can be applied using a reflow soldering method to create a strong metallurgical bond between each of stacked devices 914.

A fifth exemplary embodiment of a THV stackable semiconductor device 918 is shown in FIG. 22. The present embodiment includes multiple rows of bond pads 204 and multiple rows of via holes 902 as shown in a top view, which are appropriately connected with metal tracings 206. Each of the

via holes 902 are disposed in organic material 602 as shown. Any number of configurations of dies 202 having multiple rows of bond pads 204 and multiple rows of via holes 902 can be implemented. In addition to the present embodiment 918, another embodiment can be realized which connects the depicted half-cut outer vias 902 to bond pads 204 which are not located on the active surface of die 202, but on an additional surface, such as an additional die 202 or elsewhere as a specific implementation requires.

A sixth exemplary embodiment of a THV stackable semiconductor device 920 is shown in FIG. 23. Device 920 illustrates an additional configuration of bond pads 204, traces 206, and a series of half-cut vias 902, which are disposed on opposing sides of die 202. The dies 902 are formed in organic material 602, which is disposed on each peripheral side of die 202 as shown. In a variation of the depicted embodiment 920, a configuration can include complete vias 902.

A seventh exemplary embodiment of a THV stackable semiconductor device 922 is depicted in FIG. 24. Device 922 includes a series of dummy via holes 924 which are disposed on opposing sides of die 202 as shown. Vias 902 are disposed on the left and right hand side as shown. Dummy via holes 924 can provide for electrical connectivity through device 922 for specific applications. Dummy via holes 924 can be used to connect an additional device 922 or package using a wire-bonding process. In addition, holes 924 can act as a ground or as a conduit for input/output (I/O) signals.

Dummy holes 924 can be configured, as with vias 902, in a variety of implementations. For example, multiple rows, or full or half-cut holes 924 can be implemented. FIG. 25 illustrates one such embodiment of a device 926, which includes

a row of half-cut dummy vias 924 on the left side of die 202, and a row of THVs 902, on the right side of die 202, again disposed in organic material 602.

FIG. 26 illustrates a ninth exemplary embodiment of a THV stackable semiconductor device 928, depicting two stacked dies 202 and 203 utilizing dummy via holes 902 as shown in FIGs. 24 and 25 to connect a top die 203 with a wire-bonding process. A series of bond pads 205 is disposed on an active surface of die 203. Wire-bonds 207 connect bond pads 205 to vias 902. A dielectric, insulating or bonding material 209 is disposed between die 202 and die 203 to provide structural support for device/package 928.

Semiconductor devices, such as device 200 incorporating a series of THVs 226 or 902 can provide a variety of functionality and flexibility in various applications. Use of organic material 210 allows placement of vias 226 outside die 202, which allows for additional circuitry within die 202 and enhancing the functionality of device 200. In addition, by using organic material 210 instead of wafer 300 material, the respective yield per wafer is increased. The organic material can be configured to be as thick as needed to accommodate a variety of vias 226 in any number of applications.

Device 200 can be incorporated into a variety of package-on-package (PoP) configurations, which make use of THV 226. Such a device can include a semiconductor die having an integrated THV 226. Such a semiconductor die can be referred to as a THV die. Current package-in-package (PiP) packaging techniques make use of wire and/or bump interconnections to provide electrical signals between dies, interposers, and packages. There is growing demand to provide more robust, efficient and space saving interconnections. The use of THV

structures like 226, and thereby, THV dies to provide such interconnections can provide more robust, efficient, and space saving interconnections.

Turning to FIG. 27A, a tenth exemplary embodiment of a THV stackable semiconductor device 220 is shown. Device 220 includes die 202. An organic material 210 is disposed around peripheral surfaces 214 of die 202. The organic material is disposed along sides 218 and 216 of die 202. A bond pad 204 is formed over a top surface or integrated into a top surface of die 202. The bond pad 204 is connected to THV 226, in which a conductive material is disposed, by way of metal traces 206. A series of RDL and interconnection pads are disposed in the configuration shown above or integrated into the top surface of die 202. The RDLS and interconnection pads provide for electrical connection terminals for additional dies to be stacked over die 202.

FIG. 27B illustrates a side-view representation of the THV die configuration 220, including a second semiconductor die 224 which is stacked above THV die 202. The RDLS/pads are coupled to a series of bumps 222 to electrically connect die 224. THV die 202 incorporates THV structure 226 previously described, which is integrated into organic material 210 disposed around peripheral surfaces of die 202 as shown. A series of bond pads 204 and metal traces 206 provide an electrical path to route signals through via 226 and to the top surface of Die 202.

FIG. 28 illustrates a first exemplary embodiment 228 of a series of package-in-package (PiP) configurations which make use of the THV structure. In some cases, as in the example illustrated, the package-in-package structures are formed over circuit carrier substrate 230. In addition,

however, the underlying base material can include such structures as a leadframe. THV structures 226 can be used to connect a top integrated circuit, or a top integrated package using wires and/or bump interconnections. Vias 226 can act as ground or to route input/output (I/O) signals, as previously described.

Package 228 as illustrated includes die 202. An adhesive material such as a die attach (D/A) adhesive 209 couples die 202 to wire bond die 224. A bond pad 205 on wire bond die 224 uses wire 207 to couple die 224 to via 226 at terminal location 213. Wire bond die 224 and THV die 202 are disposed over substrate 230 having a series of bumps 232. An encapsulant 211 is formed over THV die 202 and wire bond die 224.

FIG. 29 illustrates an additional wire bond embodiment of package 234, where wire bond die 224 is instead wire-bonded to bond pads 204 integrated into the top surface of die 202. The bond pads 204 are coupled to via 226 using metal traces 206.

In a similar embodiment, FIG. 30 illustrates a wire bond embodiment of package 236, where a series of bond pads 205 allow die 224 to be wire-bonded to both via 226 at location 213, and substrate 230 at location 238.

FIG. 31 illustrates an exemplary package 238, where wire bond die 224 overhangs THV die 202, as denoted by distance arrow 240. The bond pad 205 couples die 224 directly with substrate 230.

FIG. 32 illustrates a PiP 242 where a flip chip die 244 is disposed above THV die 202 and electrically connected to the RDL/interconnection pads using bumps 248. An optional underfill material 246 is disposed between flip chip die 244

and THV die 202.

An overhanging third, wire bond die 245 is disposed above flip chip die 244 in the exemplary PiP 250 shown in FIG. 33. The overhanging wire bond die 245 is wire-bonded from bond pad 252 to via 226 at terminal 213. Again, D/A 209 adheres the overhanging die 245 to flip chip die 244.

In PiP 254, leadframe package 256 is attached to THV die 202 as shown in FIG. 34. Package 256 includes an incorporated die 258 and die paddle 260, which are attached using D/A 209. A lead terminal 262 allows wires 207 to be coupled to both bond pad 204 and via 226. Package 256 is attached to THV die 202 using D/A 209. Package 256 can include such devices as a quad flat nonlead (QFN) package, small outline nonlead (SON), and quad flat package (QFP), or similar package configurations.

The leadframe package 256 is replaced with array package 266 in FIG. 35, which illustrates exemplary PiP 264. The array package 266 also includes die 268 disposed over a substrate, whose bumps 270 couple the array package 266 to THV die 202 and to RDL/pads. Package 266 can include such devices as a land grid array (LGA), ball grid array (BGA), or similar package configurations. Again, optional underfill material 208 couples package 266 to die 202.

FIG. 36 illustrates PiP 272, which incorporates an inverted top package 274. The inverted package 274 also includes die 276 and die paddle 278. A lead terminal 282 wire-bonds package 274 to via 226. The inverted top package 274 can include such devices as a QFN, SON, QFP, LGA, BGA, or similar package configurations.

FIG. 37 illustrates another package 284 incorporating an inverted top package 286 similar to package 274. Package

286 is adhered to THV die 202 using D/A material 288. A flip chip die 244 is disposed over package 286 as shown, making use of bumps 248 and the optional underfill 246. The flip chip die 244 can include wire bond dies or additional semiconductor integrated circuit packages.

FIG. 38 illustrates a PiP 290 configuration where THV die 202 is disposed over inverted package 286 using a plurality of bumps to connect a top surface of package 286 to a bottom surface of vias 226. Again, the inverted bottom package 286 can include such devices as QFN, SON, QFP, LGA, BGA, flip chip bare dies and wafer level packages (WLPs) 286. Package 286 is attached with D/A 288 and wire-bonded to substrate 230 as shown.

FIG. 39 illustrates the configuration as shown in FIG. 38 but with additional stacking. Package 292 includes an additional flip chip die 244, which is disposed over a top surface of THV die 202 utilizing bumps 248 and underfill 246 in a manner similar to FIG. 32. Other semiconductor devices such as wire bond die can also be used in place of flip chip die 244.

Turning to FIG. 40, exemplary PiP 296 incorporates an inverted bottom package 286. In the depicted embodiment, a series of THV dies 202 are stacked, one on top of another, as shown. The bottom surface of the top THV die via 226 is coupled to the top surface of the bottom THV die via 226. The top THV die 202 is wire-bonded from via location 283 to location 213 on the adjacent THV die via.

In a similar embodiment, THV dies 202 are stacked adjacent to each other over package 286 as shown in FIG. 41. PiP 298 again incorporates the inverted bottom package 286, which is attached to substrate 230 as shown. In the depicted

embodiment, an additional flip chip die 304, or similar die 304 or integrated circuit package 304 is disposed over THV die 202 using bumps 306.

FIG. 42 illustrates a package 308 which again incorporates a bottom package 286. A solder paste 310 is coupled to the bottom surface of via 226. A passive device 312, such as an inductor, filter, capacitor, resistor, or similar passive device 312 is coupled to solder paste 310 to provide additional functionality to package 308. In the depicted embodiment, THV die 202 overhangs package 286, allowing the room for passive devices 312. An encapsulant 211 covers portions of all of the components of package 308 as shown to provide structural support. A bond pad 314 couples THV die 202 to substrate 230 at location 294.

In an additional embodiment shown in FIG. 43, PiP 316 again includes THV die 202 with attached passive devices 312 using a solder paste material 310, where devices 312 are attached to the top surface of vias 226. A bottom package 318 can again include such configurations as QFN, SON, QFP, LGA, BGA, flip chip bare dies, and WLP. A bond pad 314 couples THV die 202 through passive device 312 to the substrate using wires 207. Again, an encapsulant 211 is then provided for structural support of package 316.

As the various PiP embodiments illustrate, a variety of innovative, robust, flexible, and efficient PiP configurations can be realized using THV 226 of THV die 202.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

## Claims

What is claimed:

1. A semiconductor device, comprising:

a first semiconductor die;

an insulating material disposed around a peripheral region of the first semiconductor die including a first surface of the insulating material coplanar with a first surface of the first semiconductor die;

a conductive via formed through the insulating material with a side surface of the conductive via coplanar with a side surface of the insulating material;

a bond pad formed on the first surface of the first semiconductor die;

a conductive trace formed between the bond pad and the conductive via; and

a second semiconductor die disposed over the first surface of the first semiconductor die.

2. The semiconductor device of claim 1, further including an encapsulant deposited over the second semiconductor die and around the insulating material, wherein the encapsulant contacts the side surface of the conductive via.

3. The semiconductor device of claim 1, further including a third semiconductor die disposed over the first semiconductor die or the second semiconductor die.

4. The semiconductor device of claim 1, further including a bond wire mechanically bonded to a first surface of the

conductive via coplanar with the first surface of the first semiconductor die and the first surface of the insulating material.

5. The semiconductor device of claim 1, further including a substrate, wherein the first semiconductor die is disposed over the substrate.

6. A semiconductor device, comprising:

a first semiconductor die;

an insulating material disposed around a peripheral region of the first semiconductor die including a surface of the insulating material coplanar with a surface of the first semiconductor die;

a conductive via formed through the insulating material with a top surface, a side surface, and a bottom surface of the conductive via exposed from the insulating material;

a bond pad formed on the surface of the first semiconductor die; and

a conductive trace coupled between the conductive via and the bond pad.

7. The semiconductor device of claim 6, further including:

a second semiconductor die disposed over the first semiconductor die; and

an encapsulant deposited over the second semiconductor die and contacting the insulating material.

8. The semiconductor device of claim 7, further including a third semiconductor die disposed over the first semiconductor die or the second semiconductor die.

9. The semiconductor device of claim 8, wherein the third semiconductor die overhangs the second semiconductor die.

10. The semiconductor device of claim 7, wherein the second semiconductor die overhangs the first semiconductor die.

11. The semiconductor device of claim 7, further including a bond wire electrically coupled to the first semiconductor die or the second semiconductor die.

12. The semiconductor device of claim 6, further including an integrated passive device disposed over the first semiconductor die.

13. A semiconductor device, comprising:

a first semiconductor die;

an insulating material disposed around a peripheral region of the first semiconductor die;

a half-cut conductive via formed through the insulating material; and

a conductive layer formed on a surface of the first semiconductor die and a surface of the insulating material and coupled to the conductive via.

14. The semiconductor device of claim 13, further including

a bond pad formed over the surface of the first semiconductor die and coupled to the conductive via through the conductive layer.

15. The semiconductor device of claim 13, further including an

encapsulant deposited over the first semiconductor die and contacting the insulating material.

16. The semiconductor device of claim 13, further including a second semiconductor die disposed over the first semiconductor die.

17. The semiconductor device of claim 16, further including a third semiconductor die disposed over the first semiconductor die or the second semiconductor die.

18. The semiconductor device of claim 16, further including a bond wire electrically coupled to the first semiconductor die or the second semiconductor die.

19. A semiconductor device, comprising:

a first semiconductor die;

an insulating material disposed around a peripheral region of the first semiconductor die;

a conductive via formed through the insulating material with a side surface of the conductive via exposed at a side surface of the insulating material; and

a conductive trace formed on a surface of the first semiconductor die and extending to the conductive via.

20. The semiconductor device of claim 19, further including an encapsulant deposited over the first semiconductor die.

21. The semiconductor device of claim 19, further including a second semiconductor die disposed over the first semiconductor die.

22. The semiconductor device of claim 21, further including a third semiconductor die disposed over the first semiconductor die or the second semiconductor die.

23. The semiconductor device of claim 21, further including a bond wire electrically connected to the first semiconductor die or the second semiconductor die.