ABSTRACT

RF LDMOS ON PARTIAL SOI SUBSTRATE

In the prior art LDMOSFET devices capable of handling high power have been made by locating the source contact on the bottom surface of the device, allowing for good heat sinking, with connection to the source region being made through a sinker. However, this structure has poor high frequency characteristics. Also in the prior art, good high frequency performance has been achieved by introducing a dielectric layer immediately below the source/drain regions (SOI) but this structure has poor power handling capabilities. The present invention achieves both good high frequency behavior as well as good power capability in the same device. Instead of inserting a dielectric layer over the entire cross-section of the device, the dielectric layer is limited to being below the heavily doped section of the drain with a small amount of overlap into the lightly doped section. The structure is described in detail together with a process for manufacturing it.

FIGURE 4 IS SUGGESTED FOR PUBLICATION

This Sheet Has Been Replaced

