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PCT/US96/11477

VIDEO MULTIPLEXER

BACKGROUND

The present invention relates to video camera systems, and more particularly, to multiplexing video camera systems.

Multiple video camera systems using a multiplexer have individual coaxial cables which connect each of the individual video cameras with the multiplexer. This method of connecting video cameras requires a significant amount of cable, and labor to run the cables. Therefore, there is a need for multiple video camera systems which can operate on fewer cables.

Also, multiple video camera systems using a multiplexer must either have an expensive time-correcting multiplexer or, the cameras must be synchronized. Currently, if the cameras are to be synchronized, an individual synchronization wire must connect the individual video camera with a system controller. Therefore, there is a need for multiple video camera systems which can synchronize the video cameras without the need of an expensive time-correcting multiplexer or multiple individual synchronization wires to each camera.

SUMMARY

In one embodiment, the system includes a video camera line, a video system controller connected to the video camera line which inserts a synchronization pulse and a camera code on the video camera line, and at least one camera unit connected to the video camera line which inserts a video image signal on the video camera line in response to the camera code on the video camera line which corresponds to the particular camera unit.

In a further embodiment, the video system controller includes a timing control generating a timing signal which contains instructions to insert the synchronization pulse and the camera code on the video camera line, a synchronization pulse and camera code inserter generating a synchronization pulse and a camera code in response to receiving the timing signal from the timing controller, and a current driver inserting on the video camera line a current mode

of the synchronization pulse and the camera code upon receiving the synchronization pulse and the camera code from the synchronization pulse and camera code inserter.

In another further embodiment, the camera unit includes a camera generating an image signal, a video synchronization separator sending the synchronization pulse from the video camera line to the camera, a camera current driver converting the image signal from the camera into a video image signal being in a current mode, an enable switch inserting the video image signal from the camera current driver onto the video camera line upon receiving an enable signal, and a camera code decoder sending an enable signal to the enable switch upon sensing a camera code on the video camera line corresponding to the camera code for the associated camera unit.

In yet another further embodiment, the camera unit comprises a camera generating an image signal and a camera synchronization signal, a video synchronization separator sending the synchronization pulse from the video camera line to the camera, a video synchronization remover blanking the camera synchronization signal from the camera in response to a blanking signal from the video synchronization separator, a camera current driver converting the image signal from the camera into a video image signal being in a current mode, an enable switch inserting the video image signal from the camera current driver onto the video camera line upon receiving an enable signal, and a camera code decoder sending an enable signal to the enable switch upon sensing a camera code corresponding to the camera code for the associated camera unit.

In yet another further embodiment, the synchronization pulses inserted onto the video camera line are synchronized with the cycles of an input power supply.

In another embodiment, the system includes a video camera line, a video system controller connected to the video camera line which inserts a synchronization pulse on the video camera line, and at least one camera unit connected to the video camera line which inserts a video image signal on the video camera line in synchronization with the synchronization pulses placed on the video camera line by the video system controller.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features, aspects, and advantages of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawing where:

FIG. 1 illustrates a block diagram of one embodiment of the present invention;

FIG. 2 illustrates a frame of video having a non-viewed video line and a viewed video line;

FIG. 3 illustrates a non-viewed video line from a frame of video created by the video system controller in FIG. 1, the non-viewed video line having a synchronization pulse and a camera code therein;

FIG. 4 illustrates a viewed video line from a frame of video created by the video system controller in FIG. 1, the viewed video line having a synchronization pulse therein;

FIG. 5 illustrates a viewed video line from a frame of video generated by one of the camera units from FIG. 1, the viewed video line having a video signal and no synchronization signal;

FIG. 6 illustrates a viewed video line from a frame of video on the video cable from FIG. 1, the viewed video line having a composite of the synchronization pulse inserted into synchronization time period by the system video system controller from FIG. 1 and a video signal added to active video time period of the viewed video line by one of the camera units from FIG. 1;

FIG. 7 illustrates a block diagram of the video system controller from FIG. 1;

FIG. 8 illustrates a block diagram of one embodiment of one of the camera units from FIG. 1;

FIG. 9 illustrates a block diagram of the camera unit from FIG. 8;

FIG. 10 illustrates a block diagram of another embodiment of one of the camera units from FIG. 1;

FIG. 11 illustrates a schematic of an embodiment of a synchronization pulse insertion aspect of the video synchronization and code inserter and the current driver from the video system controller in FIG. 7; and

FIG. 12 illustrates a schematic of an embodiment of the enable switch and the current driver from the camera unit in FIG. 8 or FIG. 10.

DESCRIPTION

Referring now to the drawings, there is shown a video multiplexer system 10 illustrating one embodiment of the present invention. The video multiplexer system 10 generally comprises a video camera line or cable 100, a video system controller 200, video camera units 301, 302, 303, and 304, and a video recorder or display 400. The video camera line 100 has a first end 110 which is connected to an output 211 of the video system controller 200, and a second end 120 which is connected to an input 212 of the video system controller 200. In one embodiment of the present invention, the video camera line 100 is a single coaxial cable. The video camera units 301, 302, 303, and 304, are connected to the video camera line 100 between the first end 110 and the second end 120. A video output 213 of the video system controller 200 sends video image signals from the video system controller 200 to the video recorder or display 400.

In one embodiment of the present invention, frames of video 500 are made up of multiple video lines, including non-viewed video lines 510 and viewed video lines 520. Each of the video lines 510 and 520 in a frame of video 500 further include synchronization time periods 511 and 521, respectively, and active video time periods 512 and 522, respectively. The video system controller 200 partially creates frames of video 500 on the video camera line 100 by inserting synchronization pulses 530 on the video camera line 100 in the synchronization signal time periods 511 and 521 of the video lines 510 and 520 for the frames of video 500. In one embodiment, the video synchronization pulses 530 generated by the system video controller 200 are standard video synchronization pulses with the proper current to provide the standard video synchronization pulse amplitude to the video camera line 100. During the active video time periods 512 in the normally

non-viewed video lines 510 of the frame of video 500, the video system controller 200 also inserts camera codes 540 onto the video camera line 100. In one embodiment, the camera codes 540 comply with standard video amplitudes.

The video synchronization pulses 530 inserted on the video camera line 100 by the video system controller 200 are used by the video camera units 301, 302, 303, and 304, to remain synchronized within the video multiplexer system 10. Each of the video camera units 301, 302, 303, and 304 will generate a video image signal 550 during the active video time period 521 of the viewed video lines 520 for the frames of video 500. The camera code 540 inserted on the video camera line 100 by the video system controller 200 will correspond with one of the video camera units 301, 302, 303, and 304. Upon sensing a camera code 540 on the video camera line 100, the corresponding camera unit 301, 302, 303, or 304 will insert the video image signal 550 generated by the corresponding camera unit onto the video camera line 100 in the active video time period 522 of the viewed video line 520 for the frame of video 500. The insertion of the video image signal 550 onto the video camera line 100 will add the video image signal 550 to the synchronization pulse 530 in the viewed video line 520, resulting in a frame of video 500 having a viewed video line 520 with a composite of the synchronization pulse 530 in the synchronization time period 521 and the video image signal 550 in the active video time period 522.

The video system controller 200 receives the frame of video 500 containing the composite of the synchronization pulse 530 and the video image signal 550, at the input 212. Upon receiving the frame of video 500 containing the composite of the synchronization pulse 530 and the video image signal 550, the video system controller 200 sends the appropriate video image signal through the video output 213 to the video recorder or display 400.

In one embodiment, the video system controller 200 comprises a timing control 220, a video synchronization pulse and camera code inserter 230, a current driver 240, termination resistors 250 and 260, a buffer 270, and a resistor 280. The timing control 220 is preferably a logic device such as a microcontroller, programmable logic device, or application specific integrated circuit (ASIC) which

determines the functions of the video system controller 200. The timing control 220 generates the synchronization pulses 530 which the video multiplexer system 10 uses to synchronize the camera units 301, 302, 303, and 304, and the other components of the video multiplexer system 10. The timing control 220 can be programmed to generate the synchronization pulses 530 at a fix time period, vary the timing period at different times, varying the timing period upon sensing a change in an input condition, or to synchronize the synchronization pulses with the cycling of an input. For example, the timing control 220 can be programmed to generate the synchronization pulses in synchronization with the input power cycles, thereby synchronizing the camera units 301, 302, 303, and 304 with the input power and creating a condition known as "lock line." In a "lock line" condition, the camera units 301, 302, 303, and 304 take video images at the same cycle location for each of the input power cycles. Other electrical devices using the same electrical input power will also be at the same cycle location of each of the input power cycles when the camera units 301, 302, 303, and 304, in a "lock line" condition, take video images. Thus, the video images taken by the camera units 301, 302, 303, and 304 in a "lock line" condition will not be influenced by other electrical devices which have different conditions at different locations of the input power cycles, such as the varying color of a florescent light at each different location of an input power cycle.

The timing control 220 also generates the camera codes 540 that controls which camera unit 301, 302, 303, or 304 is active during each frame of video 500. The determination of the sequence of active camera units, or which camera unit is displayed or recorded, is determined by the timing control 220. The decision on which video camera unit is utilized may be based on a set timing mode, by monitoring alarms, or other conditions which may require the camera multiplexing to change. Therefore, the timing control 220 controls the multiplexing action of the video multiplexer system 10 by determining which camera unit 301, 302, 303, or 304, is active for each frame of video 500, and controls the operation of the entire video multiplexer system 10 based on a logic designed specifically for the application desired. The video synchronization and camera code inserter 230 and the current driver 240 convert the synchronization pulses 530 and the camera codes

540 into a current mode and inserts them into the appropriate video lines 510, 520 of the frame of video 500 on the video cable 100 through the output 211.

The frame of video 500 having the composite of the synchronization pulse 530 from the video system controller 200 and the video image signal 550 from one of the camera units 301, 302, 303, or 304, returns on the video camera line 100 to the video system controller 200 through the input 212. In one embodiment of the present invention, the composite frame of video 500 returning to the video system controller 200 also includes the camera codes 540 inserted onto the video camera line 100 by the video system controller 200. The composite frame of video passes through a buffer 270 and a resistor 280 to the video output 213 of the video system controller 200 to the video recorder or display 400. In one embodiment, the buffer 270 has a gain of two. The termination resistors 250 and 260 are connected to the first end 110 and the second end 120 of the video camera line 100, respectively, through the output 211 and input 212, respectively, of the video system controller 200. The termination resistors 250 and 260 help prevent reflection in the video camera line 100.

In one embodiment, the video camera units 301, 302, 303, or 304, are of the type of camera unit 600 which utilizes a standard camera 640. In the camera unit 600, the frames of video 500 which are inserted on the video camera line 100 by the video system controller 200 are received by a buffer 610. The buffer 610 allows the synchronization pulses 530 and the camera codes 540 placed on the video camera line 100 by the video system controller 200 to be inputted into a video synchronization separator 620 and a camera code decoder 630 of the camera unit 600 without affecting frame of video 500 on the video camera line 100. The video synchronization separator 620 reads the synchronization pulses 530 from the incoming frames of video 500 and sends those synchronization pulses 530 to a standard camera 640 and a video synchronization remover 650.

The standard camera 640 uses the synchronization pulses 530 to remain synchronized with the other camera units and components of the video multiplexer system 10. A timing generator 642 in the standard camera 640 receives the synchronization signals 530 from the video synchronization separator 620 and

generates a timing signal based on the synchronization pulse 530 in the frames of video 500. In one embodiment, the video synchronization separator 620 is a video sync separator model EL4583C, manufactured by èlantec in Milpitas, California. The timing signal(s) generated by the timing generator 642 is supplied to a clock driver 644 and a video processor 648. The clock driver 644 drives an imaging device (CCD) 646 to create an image which is sent to the video processor 648. The video processor 648 sends a video output signal, having a camera synchronization signal thereon, to the video synchronization remover 650.

The video synchronization remover 650 removes the synchronization signals normally generated by the standard camera 640 by blanking the video synchronization signals (both vertical and horizontal) from the video signal being output by the standard camera 640. Therefore, the viewed video line 520 of the frame of video 500 which is output by the video synchronization remover 650, will only have the video image signals 550 in the active time period 522. A current driver 660 converts the video signals from the video synchronization remover 650 to a current signal which is supplied to an enable switch 670.

The camera code decoder 630 reads the camera code 540 from the frame of video 500 supplied to the camera code decoder 630 by the buffer 610. In one embodiment, the camera code decoder 630 is a logic device such as a microcontroller, programmable logic device, or application specific integrated circuit (ASIC). If the camera code inserted on the video camera line 100 by the video system controller 200 corresponds to the camera unit having the camera code decoder 630, then the camera code decoder 630 transmits an enable signal to the enable switch 670. Upon receiving an enable signal from the camera code decoder 630, the enable switch 670 connects the current driver 660 with the video camera line 100, thereby inserting the video image signals from the current driver 660 onto the video camera line 100. In one embodiment, upon receiving a camera code 540 associated with the particular camera unit, the camera code decoder 630 sends the enable signal to the enable switch 670 and continues to send the enable signal to the enable switch 670 until the camera code decoder 630 receives a camera code 540 which is not associated with the particular camera unit. A person of ordinary skill

will recognize that other methods of inserting the video signals onto the video camera line 100, such as the camera code decoder 630 sending a start and stop enable signal to the enable switch 670, the enable switch 670 remaining connected between the current driver 660 and the video camera line 100 for a frame of video upon receiving a triggering enable signal from the camera code decoder 630, the enable switch 670 activating upon the absence of an enable signal from the camera code decoder 630, or the like. Therefore, when the camera code 540 in a frame of video 500 on the video camera line 100 does not correspond with the camera code required for a specific one of the camera units 600, the specific camera unit 600 will not insert a video image signal 550 onto the video camera line 100.

In another embodiment, the video camera units 301, 302, 303, or 304, are of the type of camera unit 700 which utilizes a modified camera 740. In the camera unit 700, the frames of video 500, which are inserted on the video camera line 100 by the video system controller 200, are received by a buffer 710. The buffer 710 allows the synchronization pulses 530 and the camera codes 540 placed on the video camera line 100 by the video system controller 200, to be inputted into a video synchronization separator 720 and a camera code decoder 730 of the camera unit 700 without affecting frame of video 500 on the video camera line 100. In one embodiment, the camera code decoder 730 is a logic device such as a microcontroller, programmable logic device, or application specific integrated circuit (ASIC). The video synchronization separator 720 reads the synchronization pulses 530 from the incoming frames of video 500 and sends those synchronization pulses 530 to the modified camera 740. In one embodiment, the video synchronization separator 720 is a video sync separator model EL4583C, manufactured by Elantec in Milpitas, California. The modified camera 740 differs from the standard camera 640 in that the output signal from the modified camera 740 does not have a synchronization signal. A current driver 760 converts video signal from the modified camera 740 into a current signal and supplies that current signal to the enable switch 770.

The camera code decoder 730 reads the camera code 540 from the frame of video 500 supplied to the camera code decoder 730 by the buffer 710. If the camera

code inserted on the video camera line 100 by the video system controller 200 corresponds to the camera unit having the camera decoder 730, then the camera code decoder 730 transmits an enable signal to the enable switch 770. Upon receiving an enable signal from the camera code decoder 730, the enable switch 770 inserts the video image signals from the current driver 760, onto the video camera line 100. In one embodiment, upon receiving a camera code 540 associated with the particular camera unit, the camera code decoder 730 sends the enable signal to the enable switch 770 and continues to send the enable signal to the enable switch 770 until the camera code decoder 730 receives a camera code 540 which is not associated with the particular camera unit. A person of ordinary skill will recognize that other methods of inserting the video signals onto the video camera line 100, such as the camera code decoder 730 sending a start and stop enable signal to the enable switch 770, the enable switch 770 remaining connected between the current driver 760 and the video camera line 100 for a frame of video upon receiving a triggering enable signal from the camera code decoder 730, the enable switch 770 activating upon the absence of an enable signal from the camera code decoder 730, or the like. Therefore, when the camera code 540 in a frame of video 500 on the video camera line 100 does not correspond with the camera code required for a specific one of the camera units 700, the specific camera unit 700 will not insert a video image signal 550 onto the video camera line 100.

In one embodiment, a synchronization pulse insertion aspect of the video synchronization and camera code inserter 230 and the current driver 240 of the video system controller 200 are comprised of the schematic 800. In the schematic 800, a first end 811 of a resistor R_4 receives signals from the timing control 220. A second end 812 of the resistor R_4 is connected to a base 821 of a PNP transistor T_1. An emitter 822 of the transistor T_1 is connected to a first end 841 of a resistor R_2, a first end 861 of a resistor R_E, and a positive pole of a first voltage supply V_1. A collector 823 of the transistor T_1 is connected to a first end 831 of a resistor R_3. A second end 832 of the resistor R_3 is connected to a second end 842 of the resistor R_2, a first end 851 of a resistor R_1, and a base 871 of a PNP transistor T_2. A second

end 852 of the resistor R_1 is connected to ground. An emitter 872 of the transistor T_2 is connected to a second end 862 of the resistor R_E. A collector 873 of the transistor T_2 is connected to a first end 881 of a resistor R_L, a first end 891 of a resistor R_T, and to the video camera line 100. A second end 882 of the resistor R_L is connected to a negative pole of the first voltage supply V_1. A second end 892 of the resistor R_T is connected to ground. A camera code insertion aspect of the video synchronization and camera code inserter 230 and the current driver 240 is comprised of a schematic similar to the schematic 800.

In one embodiment, the current driver 660 and the enable switch 670 of the camera unit 600, or the current driver 760 and the enable switch 770 of the camera unit 700, are comprised of the schematic 900. In the schematic 900, a base 911 of an NPN transistor T_3 receives video signals from either the video synchronization remover 650 of the camera unit 600, or the modified camera 740 of the camera unit 700. An emitter 912 of the transistor T_3 is connected to a first end of a resistor R_6. A second end 932 of the resistor R_6 is connected to ground. A collector 913 of the transistor T_3 is connected to a first end 921 of a resistor R_5 and a base 941 of an NPN transistor T_4. A second end 922 of the resistor R_5 is connected to a positive pole of a second voltage supply V_2. A collector 942 of the transistor T_4 is also connected to the positive pole of the second voltage supply V_2. An emitter 943 of the transistor T_4 is connected to a first end 991 of a resistor R_7 and a base 961 of a PNP transistor T_5. A second end 992 of the resistor R_7 is connected to ground. An emitter 962 of the transistor T_5 is connected to a first end 951 of a resistor R_8. A second end 952 of the resistor R_8 is connected to the positive pole of the second voltage supply V_2. A collector 963 of the transistor T_5 is connected to a first end of a resistor R_9 and an emitter 981 of a PNP transistor T_6. A second end 972 of the resistor R_9 is connected to a negative pole of the second voltage supply V_2. A collector 982 of the transistor T_6 connects with the video camera line 100. A base 983 of the transistor T_6 is connected to a first end 984 of a resistor R_{10}. A second end 985 of the resistor R_{10} connects with the camera code decoder 630 of the camera unit 600, or the camera code decoder 730 of the camera unit 700.

The video image signals 550 supplied by the camera unit 600 or the camera unit 700 to the video camera line 100 are without synchronization pulses and are summed with the synchronization pulses 530 provided by the video system controller 200 using current mode. Therefore, the video is "built" on the video camera line 100 by the video system controller 200 and the camera unit 301, 302, 303, or 304 selected by the video system controller 200. The video camera line 100 acts as a summing node for the current drive 240 of the video system controller 200 and the current drive 660, 760 of the camera unit 600, 700.

Since the camera units 301, 302, 303, and 304 and the video controller 200 interface to the video camera line 100 through a current mode, the video camera line 100 acts as a summing node allowing an unlimited number of cameras to be placed on the video camera line 100. Since the video synchronization pulses 530 are placed on the video camera line 100 by the video system controller 200, all of the camera units 301, 302, 303, and 304 use the same synchronization pulses 530 on the video camera line 100 to synchronize themselves to the video system controller 200 without the use of separate synchronization wires. Also, because the video camera line 100 acts as the summing node for the multiplexer, the camera units 301, 302, 303, and 304 do not need separate multiplexing cables to connect with a multiplexer. Furthermore, the video system controller 200 which can be programmed to multiplex the camera units 301, 302, 303, and 304 according to many different parameters which are programed into the video system controller 200.

Although the present invention has been described in considerable detail with reference to certain preferred embodiments thereof, other embodiments are possible. For example, the video cable 100 can be a single line with many branches for the individual cameras, with the input and output connected to the same base location of the trunk of the single line. As another example, other arrangements of camera components can be utilized which will generate only the video signal to be inserted in blank frames generated by the signal controller. Therefore, the spirit and scope of the appended claims should not be limited to the description of the preferred embodiment contained herein.

WHAT IS CLAIMED IS:

1. A system for video multiplexing comprising:

a video camera line;

a video system controller connected to said video camera line, wherein said video controller inserts a synchronization pulse and a camera code on said video camera line;

a camera unit connected to said video camera line, wherein said camera unit inserts a video image signal on said video camera line in response to the camera code inserted on said video camera line by said video system controller, and wherein said camera unit uses the synchronization pulse inserted on said video camera line by said video system controller to synchronize the video image signal.

2. The system for video multiplexing according to claim 1, wherein said video system controller further comprises:

a timing control, said timing control generating a timing signal containing instructions to insert the synchronization pulse and the camera code;

a synchronization pulse and camera code inserter connected to said timing control, said generating a synchronization pulse and a camera code in response to receiving the timing signal from said timing control;

a current driver connected to said synchronization pulse and camera code inserter, said current driver inserting on said video camera line a current mode of the synchronization pulse and the camera code upon receiving the synchronization pulse and the camera code from said synchronization pulse and camera code inserter.

3. The system for video multiplexing according to claim 1, wherein the camera unit further comprises:

a camera, said camera generating an image signal;

a video synchronization separator connected to said camera, said video synchronization separator sending the synchronization pulse from said video camera line to said camera, wherein said camera uses the synchronization pulse to synchronize the image signal generated by said camera;

a camera current driver connected to said camera, said camera current driver converting said image signal from said camera into a video image signal being in a current mode;

an enable switch connected to said camera current driver, said enable switch inserting the video image signal from said camera current driver onto said video camera line upon receiving and enable signal; and

a camera code decoder connected to said enable switch, said camera code decoder sending an enable signal to said enable switch upon sensing the camera code on said video camera line.

4. The system for video multiplexing according to claim 1, wherein said camera unit further comprises:

a camera, said camera generating an image signal and a camera synchronization signal;

a video synchronization separator connected to said camera, said video synchronization separator sending the synchronization pulse from said video camera line to said camera, wherein said camera uses the synchronization pulse to synchronize the image signal generated by said camera;

a video synchronization remover connected to said camera and said video synchronization separator, said video synchronization remover blanking the camera synchronization signal from said camera in response to receiving the synchronization pulse from said video synchronization separator;

a camera current driver connected to said video synchronization remover, said camera current driver converting said image signal from said camera into a video image signal being in a current mode;

an enable switch connected to said camera current driver, said enable switch inserting the video image signal from said camera current driver onto said video camera line upon receiving and enable signal; and

a camera code decoder connected to said enable switch, said camera code decoder sending an enable signal to said enable switch upon sensing the camera code on said video camera line.

5. The system for video multiplexing according to claim 1, wherein said video system controller inserts the synchronization pulse on said video camera line such that the synchronization pulse is synchronized with an alternating current input power supply.

6. A system for video multiplexing comprising:

a video camera line;

a video system controller connected to said video camera line, wherein said video system controller, wherein said video controller inserts a synchronization pulse and one of a plurality of camera codes on said video camera line; and

a plurality of camera units, each one of said plurality of cameras associated with a different one of the plurality of camera codes of said video system controller, wherein each particular one of said plurality of camera units inserts a video image signal on said video camera line upon sensing the camera code on said video camera line which is associated with the particular one of said plurality of camera units, and wherein each particular one of said plurality of camera units synchronizes the video image signals generated by each particular one of said plurality of cameras with the synchronization pulse inserted on said video camera line by said video system controller.

7. The system for video multiplexing according to claim 6, wherein said video system controller further comprises:

a timing control, said timing control generating a timing signal containing instructions to insert the synchronization pulse and a particular one of the plurality of camera codes;

a synchronization pulse and camera code inserter connected to said timing control, said generating the synchronization pulse and the particular one of the plurality of camera codes in response to receiving the timing signal from said timing control;

a current driver connected to said synchronization pulse and camera code inserter, said current driver inserting on said video camera line a current mode of the synchronization pulse and the camera code upon receiving the synchronization pulse and the camera code from said synchronization pulse and camera code inserter.

8. The system for video multiplexing according to claim 6, wherein at least one of said plurality of camera units further comprises:

a camera, said camera generating an image signal;

a video synchronization separator connected to said camera, said video synchronization separator sending the synchronization pulse from said video camera line to said camera, wherein said camera uses the synchronization pulse to synchronize the image signal generated by said camera;

a camera current driver connected to said camera, said camera current driver converting said image signal from said camera into a video image signal being in a current mode;

an enable switch connected to said camera current driver, said enable switch inserting the video image signal from said camera current driver onto said video camera line upon receiving and enable signal; and

a camera code decoder connected to said enable switch, said camera code decoder sending an enable signal to said enable switch upon sensing on the video camera line the particular one of said plurality of camera codes associated with the at camera unit.

9. The system for video multiplexing according to claim 6, wherein at least one of said plurality of camera units further comprises:

a camera, said camera generating an image signal and a camera synchronization signal;

a video synchronization separator connected to said camera, said video synchronization separator sending the synchronization pulse from said video camera line to said camera, wherein said camera uses the synchronization pulse to synchronize the image signal generated by said camera;

a video synchronization remover connected to said camera and said video synchronization separator, said video synchronization remover blanking the camera synchronization signal from said camera in response to receiving the synchronization pulse from said video synchronization separator;

a camera current driver connected to said video synchronization remover, said camera current driver converting said image signal from said camera into a video image signal being in a current mode;

an enable switch connected to said camera current driver, said enable switch inserting the video image signal from said camera current driver onto said video camera line upon receiving and enable signal; and

a camera code decoder connected to said enable switch, said camera code decoder sending an enable signal to said enable switch upon sensing on the video camera line the particular one of said plurality of camera codes associated with the camera unit.

10. The system for video multiplexing according to claim 6, wherein said video system controller inserts the synchronization pulse on said video camera line such that the synchronization pulse is synchronized with an alternating current input power supply.

11. A system for video multiplexing comprising:

a video camera line;

a video system controller connected to said video camera line, wherein said video controller inserts a synchronization pulse on said video camera line;

a camera unit connected to said video camera line, wherein said camera unit inserts a video image signal on said video camera line, and wherein said camera unit uses the synchronization pulse inserted on said video camera line by said video system controller to synchronize the video image signal.