

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based on and claims priority from Korean Patent Application No. 10-2021-0123719 filed on 16 September 2021 in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

TECHNICAL FIELD

[0002] The present disclosure relates to a semiconductor device and a method for manufacturing the same.

BACKGROUND

[0003] Although a voltage decreases with miniaturization of semiconductor elements, there are cases where a booster circuit is provided inside or a power supply voltage itself is about 12V, of which an example is a vehicle application. In order to cope with such application, it is generally performed to form a high voltage transistor together with a low voltage transistor inside one same semiconductor element. In the process of forming the low voltage transistor and the high voltage transistor inside the same semiconductor element, there is a problem that heights of gate electrodes are formed non-uniformly.

SUMMARY

[0004] Various embodiments of the present disclosure provide a semiconductor device and a method for manufacturing a semiconductor that may enable a low voltage transistor, an intermediate voltage transistor, and a high voltage transistor formed on a same substrate to have respective gate electrodes having a same thickness and respective gate

insulating layers having different thicknesses, thereby to be formed at a same level on the substrate.

[0005] According to an embodiment, there is provided a semiconductor device that may include: a substrate including first and second regions thereon; a first active region in the first region; an active pattern protruding from the first active region; a second active region in the second region; a first gate electrode on the active pattern; a second gate electrode on the second active region; a first gate insulating layer, including a first-first insulating layer, between the active pattern and the first gate electrode; and a second gate insulating layer, including a second-first insulating layer and a second-second insulating layer below the second-first insulating layer, between the second active region and the second gate electrode, wherein a thickness in a vertical direction of the first gate electrode that overlaps the active pattern in the vertical direction is equal to a thickness in the vertical direction of the second gate electrode that overlaps the second active region in the vertical direction, and an upper surface of the first gate electrode is formed at a same level as an upper surface of the second gate electrode.

[0006] According to an exemplary embodiment, there is provided a semiconductor device that may include: a substrate including first to third regions thereon; a first active region in the first region; an active pattern protruding from the first active region; a second active region in the second region; a third active region in the third region; a first gate electrode on the active pattern; a second gate electrode on the second active region; a third gate electrode on the third active region; a first gate insulating layer, including a first-first insulating layer, between the active pattern and the first gate electrode; and a second gate insulating layer, including a second-first insulating layer and a second-second insulating layer below the second-first insulating layer, between the second active region and the second gate

electrode; and a third gate insulating layer, including a third-first insulating layer, a third-second insulating layer below the third-first insulating layer, and a third-third insulating layer below the third-second insulating layer, between the third active region and the third gate electrode, wherein a thickness in a vertical direction of the first gate electrode that overlaps the active pattern in the vertical direction, a thickness in the vertical direction of the second gate electrode that overlaps the second active region in the vertical direction, and a thickness in the vertical direction of the third gate electrode that overlaps the third active region in the vertical direction are equal to one another, and wherein an upper surface of the first gate electrode, an upper surface of the second gate electrode, and an upper surface of the third gate electrode are formed at a same level on the substrate.

[0007] According to an exemplary embodiment, there is provided a method for fabricating a semiconductor device. The method may include: providing a substrate including first to third regions thereon; etching an upper surface of the substrate at the second region to form a first trench, and etching the upper surface of the substrate at the third region to form a second trench; forming a first insulating material layer inside each of the first and second trenches; etching the substrate at the first region to form an active pattern; etching the substrate at each of the first to third regions to form first to third active regions; etching at least a part of the first insulating material layer formed on the third active region; forming a second insulating material layer on the third active region; etching the first insulating material layer formed on the second active region; forming a third insulating material layer on each of the second active region and the second insulating material layer of the third active region; forming an insulating layer on each of the active pattern, the third insulating material layer formed on the second active region, and the third insulating material layer formed on the third active region; and forming a first gate electrode on the insulating layer on the active pattern, forming a second gate electrode on the insulating layer on the second active region, and

forming a third gate electrode on the insulating layer on the third active region, wherein a thickness in a vertical direction of the first gate electrode that overlaps the active pattern in the vertical direction, a thickness in the vertical direction of the second gate electrode that overlaps the second active region in the vertical direction, and a thickness in the vertical direction of the third gate electrode that overlaps the third active region in the vertical direction are equal to one another, and wherein an upper surface of the first gate electrode, an upper surface of the second gate electrode, and an upper surface of the third gate electrode are formed at a same level.

[0008] However, aspects are not restricted to the one set forth herein. The above and other aspects will become more apparent to one of ordinary skill in the art to which the present disclosure pertains by referencing the detailed description given below.

BRIEF DESCRIPTION OF DRAWINGS

[0009] The above and other aspects and features of the present disclosure will become more apparent by describing in detail exemplary embodiments thereof referring to the attached drawings, in which:

[0010] FIG. 1 is a schematic layout diagram for explaining a semiconductor device according to embodiments;

[0011] FIG. 2 is a cross-sectional view taken along each of line A-A', line B-B', line C-C' and line D-D' of FIG. 1;

[0012] FIGS. 3 to 20 are intermediate stage diagrams for explaining a method for fabricating a semiconductor device, according to embodiments;

[0013] FIGS. 21 to 27 are intermediate stage diagrams for explaining a method for fabricating a semiconductor device, according to embodiments;

[0014] FIG. 28 is a cross-sectional view for explaining a semiconductor device, according to embodiments;

[0015] FIGS. 29 to 32 are intermediate stage diagrams for explaining a method for fabricating a semiconductor device, according to embodiments; and

[0016] FIG. 33 is a cross-sectional view for explaining a semiconductor device, according to embodiments.

DETAILED DESCRIPTION

[0017] The embodiments described herein are example embodiments, and thus, the inventive concept is not limited thereto and may be realized in various other forms.

[0018] It will be understood that when an element or layer is referred to as being "over," "above," "on," "below," "under," "beneath," "connected to" or "coupled to" another element or layer, it can be directly over, above, on, below, under, beneath, connected or coupled to the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly over," "directly above," "directly on," "directly below," "directly under," "directly beneath," "directly connected to" or "directly coupled to" another element or layer, there are no intervening elements or layers present.

[0019] It will be understood that, although the terms first, second, third, fourth, first-first, first-second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present

inventive concept.

[0020] As used herein, expressions such as “at least one of,” when preceding a list of elements, modify the entire list of elements and do not modify the individual elements of the list. For example, the expression, "at least one of a, b, and c," should be understood as including only a, only b, only c, both a and b, both a and c, both b and c, or all of a, b, and c.

[0021] Although drawings of a semiconductor device according to some embodiments illustrate a fin-type transistor (FinFET) having a channel region of a fin-type pattern shape as an example, the present disclosure is not limited thereto. In some other embodiments, the corresponding semiconductor device may include a MBCFETTM (Multi-Bridge Channel Field Effect Transistor) having nanosheets as its channel region.

[0022] Hereinafter, a semiconductor device according to embodiments will be described referring to FIGS. 1 and 2.

[0023] FIG. 1 is a schematic layout diagram for explaining a semiconductor device, according to some embodiments. FIG. 2 is a cross-sectional view taken along each of line A-A', line B-B', line C-C' and line D-D' of FIG. 1.

[0024] Referring to FIGS. 1 and 2, the semiconductor device according to embodiments includes a substrate 100, a field insulating layer 105, first to third gate electrodes G1, G2 and G3, first to third gate insulating layers, first to third gate spacers 121, 122 and 123, first to third capping patterns 131, 132 and 133, first to third source/drain regions SD1, SD2 and SD3, a first interlayer insulating layer 140, an etching stop layer 150, and a second interlayer insulating layer 160.

[0025] The substrate 100 may be a silicon substrate or an SOI (silicon-on-insulator). In contrast, the substrate 100 may include, but is not limited to, silicon germanium, SGOI (silicon germanium on insulator), indium antimonide, lead tellurium compounds, indium

arsenic, indium phosphide, gallium arsenide or gallium antimonide. However, the present disclosure is not limited thereto.

[0026] First to third regions I, II and III may be defined on the substrate 100.

According to an embodiment, a low voltage transistor may be disposed on the substrate 100 at the first region I, an intermediate voltage transistor may be disposed on the substrate 100 at the second region II, and a high voltage transistor may be disposed on the substrate 100 at the third region III.

[0027] Each of first to third active regions AR1, AR2, and AR3 may extend in a first horizontal direction DR1 on the substrate 100. Each of the first to third active regions AR1, AR2, and AR3 may protrude from the substrate 100 in a vertical direction DR3. Each of the first to third active regions AR1, AR2, and AR3 may be a part of the substrate 100, or may be or may include an epitaxial layer that is grown from the substrate 100.

[0028] The first active region AR1 may be disposed in the first region I, the second active region AR2 may be disposed on the second region II, and the third active region AR3 may be disposed in the third region III. The first active region AR1 may be defined by a first deep trench DT1 formed in the first region I. The second active region AR2 may be defined by a second deep trench DT2 formed in the second region II. The third active region AR3 may be defined by a third deep trench DT3 formed in the third region III.

[0029] First and second active patterns F1 and F2 may be formed to extend in the first horizontal direction DR1 on the first active region AR1. Each of the first and second active patterns F1 and F2 may protrude from the first active region AR1 in the vertical direction DR3. The second active pattern F2 may be spaced apart from the first active pattern F1 in a second horizontal direction DR2 different from the first horizontal direction DR1. Each of the first and second active patterns F1 and F2 may function as a channel structure of a

corresponding transistor formed in the first region I.

[0030] According to an embodiment, an upper surface of the second active region AR2 may be formed at a level lower than an upper surface of a first active pattern F1. The upper surface of the second active region AR2 may be formed at a level between the upper surface of the first active region AR1 and the upper surface of the first active pattern F1. An upper surface of the third active region AR3 may be formed at a level lower than the upper surface of the second active region AR2. Upper portions of the first and second active regions AR2 and AR3 may function as channel structures of corresponding transistors formed in the second and third regions II and III, respectively.

[0031] The field insulating layer 105 may be disposed on the substrate 100. The field insulating layer 105 may surround side walls of each of the first to third active regions AR1, AR2, and AR3. The field insulating layer 105 may surround side walls of each of the first and second active patterns F1 and F2. Each of the first and second active patterns F1 and F2 may protrude above a level of an upper surface of the field insulating layer 105 in the vertical direction DR3. The field insulating layer 105 may include, for example, an oxide film, a nitride film, an oxynitride film or a combination film thereof.

[0032] A first gate electrode G1 may extend in a second horizontal direction DR2 on the first active region AR1. The first gate electrode G1 may be disposed on the first and second active patterns F1 and F2. A second gate electrode G2 may extend in the second horizontal direction DR2 on the second active region AR2. A third gate electrode G3 may extend in the second horizontal direction DR2 on the third active region AR3.

[0033] Thicknesses of the first to third gate electrodes G1, G2, and G3 in the vertical direction DR3 may be equal to one another. For example, a first thickness t_1 in the vertical direction DR3 of the first gate electrode G1 that overlaps the first active pattern F1 in the

vertical direction DR3, a second thickness t_2 in the vertical direction DR3 of the second gate electrode G2 that overlaps the second active region AR2 in the vertical direction DR3, and a third thickness t_3 in the vertical direction DR3 of the third gate electrode G3 that overlaps the third active region AR3 in the vertical direction DR3 may be equal to one another.

[0034] Upper surfaces of the first to third gate electrodes G1, G2, and G3 may be formed at a same level on the substrate 100. For example, an upper surface G1u of the first gate electrode G1 that is in contact with a bottom surface of a first capping pattern 131, an upper surface G2u of the second gate electrode G2 that is in contact with a bottom surface of a second capping pattern 132, and an upper surface G3u of the third gate electrode G3 that is in contact with a bottom surface of a third capping pattern 133 may be formed at a same level on the substrate 100.

[0035] Each of the first to third gate electrodes G1, G2, and G3 may include, for example, at least one of titanium nitride (TiN), tantalum carbide (TaC), tantalum nitride (Ta₂N₃), titanium silicon nitride (TiSiN), tantalum silicon nitride (TaSiN), tantalum titanium nitride (TaTiN), titanium aluminum nitride (TiAlN), tantalum aluminum nitride (TaAlN), tungsten nitride (WN), ruthenium (Ru), titanium aluminum (TiAl), titanium aluminum carbonitride (TiAlC-N), titanium aluminum carbide (TiAlC), titanium carbide (TiC), tantalum carbonitride (TaCN), tungsten (W), aluminum (Al), copper (Cu), cobalt (Co), titanium (Ti), tantalum (Ta), nickel (Ni), platinum (Pt), nickel platinum (Ni-Pt), niobium (Nb), niobium nitride (NbN), niobium carbide (NbC), molybdenum (Mo), molybdenum nitride (MoN), molybdenum carbide (MoC), tungsten carbide (WC), rhodium (Rh), palladium (Pd), iridium (Ir), osmium (Os), silver (Ag), gold (Au), zinc (Zn), vanadium (V), and combinations thereof. Each of the first to third gate electrodes G1, G2, and G3 may include a conductive metal oxide, a conductive metal oxynitride, and the like, and may

include a form in which the above-mentioned substance is oxidized.

[0036] A first source/drain region SD1 may be disposed on at least one side of the first gate electrode G1. The first source/drain region SD1 may be disposed on each of the first and second active patterns F1 and F2. A second source/drain region SD2 may be disposed on at least one side of the second gate electrode G2. The second source/drain region SD2 may be disposed on the second active region AR2. A third source/drain region SD3 may be disposed on at least one side of the third gate electrode G3. The third source/drain region SD3 may be disposed on the third active region AR3.

[0037] According to an embodiment, an upper surface of the second source/drain region SD2 may be formed at a level lower than the upper surface of the first source/drain region SD1. An upper surface of the third source/drain region SD3 may be formed at a level lower than the upper surface of the second source/drain region SD2. According to an embodiment, a thickness of the third source/drain region SD3 in the vertical direction DR3 may be greater than a thickness of the second source/drain region SD2 in the vertical direction DR3.

[0038] A first gate spacer 121 may extend in the second horizontal direction DR2 along both side walls of the first gate electrode G1. A second gate spacer 122 may extend in the second horizontal direction DR2 along both side walls of the second gate electrode G2. A third gate spacer 123 may extend in the second horizontal direction DR2 along both side walls of the third gate electrode G3.

[0039] Each of the first to third gate spacers 121, 122 and 123 may include, for example, at least one of silicon nitride (SiN), silicon oxynitride (SiON), silicon oxide (SiO₂), silicon oxycarbonitride (SiOCN), silicon boronitride (SiBN), silicon oxyboronitride (SiOBN), silicon oxycarbide (SiOC), and combinations thereof

[0040] In the first region I, the first gate insulating layer 111 may include a first insulating layer 111. The first gate insulating layer 111 may be formed of a single film including the first insulating layer 111. The first gate insulating layer 111 may be disposed between the first gate spacers 121.

[0041] In the first region I, the first insulating layer 111 may be disposed along side walls and a bottom surface of the first gate electrode G1. According to an embodiment, the first insulating layer 111 may be disposed between the first active pattern F1 and the first gate electrode G1. The first insulating layer 111 may be disposed between the field insulating layer 105 and the first gate electrode G1. The first insulating layer 111 may be disposed between the first gate spacer 121 and the first gate electrode G1.

[0042] In the second region II, the second gate insulating layers 111 and 112 may include a second insulating layer 112 and the first insulating layer 111 disposed on the second insulating layer 112. The first insulating layer 111 may be disposed along side walls and a bottom surface of the second gate electrode G2. The second gate insulating layers 111 and 112 may be disposed between the second gate spacers 122.

[0043] According to an embodiment, in the second region II, the first insulating layer 111 may be disposed between the second active region AR2 and the second gate electrode G2. The first insulating layer 111 may be disposed between the second gate spacer 122 and the second gate electrode G2. According to an embodiment, the second insulating layer 112 may be disposed between the second active region AR2 and the first insulating layer 111.

[0044] According to an embodiment, in the second region II, a width of the second insulating layer 112 in the first horizontal direction DR1 may be equal to a width of the first insulating layer 111 in the first horizontal direction DR1. According to an embodiment, a thickness of the second insulating layer 112 in the vertical direction DR3 may be greater than

a thickness of the first insulating layer 111 in the vertical direction DR3.

[0045] In the third region III, the third gate insulating layers 111, 112 and 113 may include a first insulating layer 111, a second insulating layer 112, and a third insulating layer 113. The first insulating layer 111 may be disposed along side walls and a bottom surface of the third gate electrode G3. The third gate insulating layers 111, 112 and 113 may be disposed between the third gate spacers 123.

[0046] According to an embodiment, in the third region III, the first insulating layer 111 may be disposed between the third active region AR3 and the third gate electrode G3. The first insulating layer 111 may be disposed between the third gate spacer 123 and the third gate electrode G3. According to an embodiment, the second insulating layer 112 may be disposed between the third active region AR3 and the first insulating layer 111. According to an embodiment, the third insulating layer 113 may be disposed between the third active region AR3 and the second insulating layer 112.

[0047] According to an embodiment, a width of the third insulating layer 113 in the first horizontal direction DR1 may be equal to each of a width of the second insulating layer 112 in the first horizontal direction DR1 and a width of the first insulating layer 111 in the first horizontal direction DR1. According to an embodiment, a thickness of the third insulating layer 113 in the vertical direction DR3 may be greater than a thickness of the second insulating layer 112 in the vertical direction DR3.

[0048] The first insulating layer 111 may include, for example, at least one of silicon oxide (SiO₂), silicon oxynitride (SiON), silicon nitride (SiN) and a high dielectric constant material having a dielectric constant greater than that of silicon oxide (SiO₂). The high dielectric constant material may include, for example, one or more of hafnium oxide, hafnium silicon oxide, hafnium aluminum oxide, lanthanum oxide, lanthanum aluminum oxide,

zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide and lead zinc niobate.

[0049] Each of the second insulating layer 112 and the third insulating layer 113 may include, for example, silicon oxide (SiO_2). In some other embodiments, each of the second insulating layer 112 and the third insulating layer 113 may include silicon oxynitride (SiON), silicon nitride (SiN), or a high dielectric constant material having a higher dielectric constant than silicon oxide (SiO_2).

[0050] The first capping pattern 131 may be disposed on the first gate electrode G1, the first insulating layer 111, and the first gate spacer 121. The first capping pattern 131 may extend in the second horizontal direction DR2. The second capping pattern 132 may be disposed on the second gate electrode G2, the first insulating layer 111, and the second gate spacer 122. The second capping pattern 132 may extend in the second horizontal direction DR2. The third capping pattern 133 may be disposed on the third gate electrode G3, the first insulating layer 111, and the third gate spacer 123. The third capping pattern 133 may extend in the second horizontal direction DR2.

[0051] Each of the first to third capping patterns 131, 132 and 133 may include, for example, at least one of silicon nitride (SiN), silicon oxynitride (SiON), silicon oxide (SiO_2), silicon carbonitride (SiCN), silicon oxycarbonitride (SiOCN), and combinations thereof.

[0052] The first interlayer insulating layer 140 may be disposed on the field insulating layer 105. The first interlayer insulating layer 140 may be disposed on each of the first to third source/drain regions SD1, SD2 and SD3, and the first to third gate spacers 121, 122 and 123. According to an embodiment, an upper surface of the first interlayer insulating layer 140 may be formed at a same level as upper surfaces of the first to third capping patterns 131,

132 and 133 on the substrate 100.

[0053] The first interlayer insulating layer 140 may include, for example, at least one of silicon oxide, silicon nitride, silicon oxycarbide, silicon oxynitride, silicon oxycarbonitride, and a low dielectric constant material. The low dielectric constant material may include, for example, Fluorinated TetraEthylOrthoSilicate (FTEOS), Hydrogen SilsesQuioxane (HSQ), Bis-benzoCycloButene (BCB), TetraMethylOrthoSilicate (TMOS), OctaMethyleyCloTetraSiloxane (OMCTS), HexaMethylDiSiloxane (HMDS), TriMethylSilyl Borate (TMSB), DiAcetoxyDitertiaryButoSiloxane (DADBS), TriMethylSilil Phosphate (TMSP), PolyTetraFluoroEthylene (PTFE), TOSZ (Tonen SilaZen), FSG (Fluoride Silicate Glass), polyimide nanofoams such as polypropylene oxide, CDO (Carbon Doped silicon Oxide), OSG (Organo Silicate Glass), SiLK, Amorphous Fluorinated Carbon, silica aerogels, silica xerogels, mesoporous silica or combinations thereof. However, the present disclosure is not limited thereto.

[0054] An etching stop layer 150 may be disposed on each of the first interlayer insulating layer 140 and the first to third capping patterns 131, 132 and 133. Although FIG. 2 shows that the etching stop layer 150 is formed as a single film, the present disclosure is not limited thereto. In some other embodiments, the etching stop layer 150 may be formed as multiple films. The etching stop layer 150 may include, for example, at least one of silicon oxide, silicon nitride, silicon oxyoxide, and a low dielectric constant material.

[0055] The second interlayer insulating layer 160 may be disposed on the etching stop layer 150. The second interlayer insulating layer 160 may include, for example, at least one of a silicon oxide, a silicon nitride, a silicon oxynitride, and a low dielectric constant material.

[0056] Hereinafter, a method for fabricating a semiconductor device according to some embodiments will be described referring to FIGS. 2 to 20.

[0057] FIGS. 3 to 20 are intermediate stage diagrams for explaining the method for fabricating the semiconductor device shown in FIGS. 1 and 2, according to embodiments.

[0058] Referring to FIG. 3, a substrate 100 in which first to third regions I, II and III are defined may be provided. Subsequently, a first mask pattern M1 may be formed on an upper surface of the substrate 100. Subsequently, a first trench TR1 may be formed, by etching the upper surface of the substrate 100 at the second region II, using the first mask pattern M1 as a mask. Further, a second trench TR2 may be formed, by etching the upper surface of the substrate 100 at the third region III, using the first mask pattern M1 as a mask. According to an embodiment, the first trench TR1 and the second trench TR2 may be formed to have an equal depth. That is, a lower surface of the first trench TR1 and a lower surface of the second trench TR2 may be formed at a same level on the substrate 100.

[0059] Referring to FIG. 4, a first insulating material layer 10 may be formed inside each of the first trench TR1 and the second trench TR2. The first insulating material layer 10 may include, for example, silicon oxide (SiO_2). After that, the first mask pattern M1 may be removed through a flattening process. As a result, the upper surface of the substrate 100 and an upper surface of the first insulating material layer 10 may be coplanar.

[0060] Referring to FIG. 5, a second mask pattern M2 may be formed on the upper surface of the substrate 100 and the first insulating material layer 10. Subsequently, by etching a part of the substrate 100 at the first region I using the second mask pattern M2 as a mask, the first and second active patterns F1 and F2 extending in the first horizontal direction DR1 may be formed.

[0061] Referring to FIG. 6, the field insulating layer 105 may be formed to surround the side walls of each of the first and second active patterns F1 and F2 and side walls of the second mask pattern M2. According to an embodiment, an upper surface of the field

insulating layer 105 may be formed on a same plane as an upper surface of the second mask pattern M2.

[0062] Referring to FIG. 7, a third mask pattern M3 may be formed on the field insulating layer 105 and the second mask pattern M2. Subsequently, a part of the second mask pattern M2, a part of the first insulating material layer 10, a part of the field insulating layer 105, and a part of the substrate 100 may be etched, using the third mask pattern M3 as a mask. Through this etching process, the first deep trench DT1 may be formed on the substrate 100 at the first region I, the second deep trench DT2 may be formed on the substrate 100 at the second region II, and the third deep trench DT3 may be formed on the substrate 100 at the third region III.

[0063] As a result, the first active region AR1 defined by the first deep trench DT1 may be formed on the substrate 100 at the first region I, the second active region AR2 defined by the second deep trench DT2 may be formed on the substrate 100 at the second region II, and the third active region AR3 defined by the third deep trench DT3 may be formed on the substrate 100 at the third region III. Each of the first to third active regions AR1, AR2, and AR3 may extend in the first horizontal direction DR1.

[0064] Referring to FIG. 8, the field insulating layer 105 may be further formed inside each of the first to third deep trenches DT1, DR2, and DR3. Subsequently, the third mask pattern M3 and the second mask pattern M2 may be removed through a flattening process. As a result, upper surfaces of each of the first and second active patterns F1 and F2, the upper surface of the field insulating layer 105, and the upper surface of the first insulating material layer 10 may be formed at a same level on the substrate 100.

[0065] Referring to FIG. 9, a fourth mask pattern M4 may be formed in the first region I and the second region II. Subsequently, a part of the field insulating layer 105

formed in the third region III and the first insulating material layer 10 may be etched using the fourth mask pattern M4 as a mask. For example, the first insulating material layer 10 formed in the third region III may be completely etched.

[0066] Referring to FIG. 10, the second insulating material layer 20 may be formed on the third active region AR3. According to an embodiment, a part of an upper part of the third active region AR3 may be oxidized to form the second insulating material layer 20. The second insulating material layer 20 may include, for example, a silicon oxide (SiO_2).

[0067] Referring to FIG. 11, a first protective layer 30 may be formed in the first region I and the third region III. The first protective layer 30 may expose a part of the second insulating material layer 20 formed in the third region III.

[0068] Subsequently, the fourth mask pattern M4, a part of the field insulating layer 105, and the first insulating material layer 10 formed in the second region II may be etched, using the first protective layer 30 as a mask. For example, the first insulating material layer 10 formed in the second region II may be completely etched. Further, an implant trench IT may be formed by etching a part of the second insulating material layer 20 exposed in the third region III using the first protective layer 30 as a mask. The upper surface of the third active region AR3 may be exposed through the implant trench IT.

[0069] Referring to FIG. 12, a second source/drain region SD2 may be formed in the second active region AR2. Further, a third source/drain region SD3 may be formed in the third active region AR3 through the implant trench IT. Subsequently, the first protective layer 30 may be removed. According to an embodiment, a thickness of the third source/drain region SD3 in the vertical direction DR3 may be formed to be greater than a thickness of the second source/drain region SD2 in the vertical direction DR3.

[0070] Referring to FIG. 13, a third insulating material layer 40 may be formed in the

first to third regions I, II and III. For example, the third insulating material layer 40 may be conformally formed. For example, an upper surface of the third insulating material layer 40 formed in the second and third regions II and III may be formed at a same level as the upper surface of the first active pattern F1. The third insulating material layer 40 may include, for example, silicon oxide (SiO_2).

[0071] Referring to FIG. 14, the third insulating material layer 40 formed in the first region I may be removed. Subsequently, a fifth mask pattern M5 may be formed on the fourth mask pattern M4 in the first region I and the third insulating material layer 40 in the second and third regions II and III.

[0072] Referring to FIG. 15, a second protective layer 50 may be formed on the fifth mask pattern M5 in the second and third regions II and III. Subsequently, the fifth mask pattern M5 and the fourth mask pattern M4 in the first region I may be etched, using the second protective layer 50 as a mask. Further, a part of the field insulating layer 105 may be etched to expose an upper portion of each of the first and second active patterns F1 and F2.

[0073] Referring to FIG. 16, the second protective layer 50 and the fifth mask pattern M5 in the second and third regions II and III may be removed. Subsequently, a dummy gate material layer DGM may be formed on the first and second active patterns F1 and F2 in the first region I, the field insulating layer 105 in the first region I, and the third insulating material layer 40 in the second and third regions II and III.

[0074] Referring to FIG. 17, a sixth mask pattern M6 may be formed on the dummy gate material layer DGM. Next, the dummy gate material layer DGM may be etched, using the sixth mask pattern M6 as a mask. Through this etching process, a plurality of dummy gates DG extending in the second horizontal direction DR2 may be formed in each of the first to third regions I, II and III.

[0075] The third insulating material layer 40 in the second region II may be etched while the plurality of dummy gates DG are formed. The remaining unetched third insulating material layer 40 may be defined as a second insulating layer 112. Further, the third insulating material layer 40 and the second insulating material layer 20 in the third region III may be etched while the plurality of dummy gates DG are formed. The unetched third insulating material layer 40 in the third region III may also be defined as a second insulating layer 112, and the unetched second insulating material layer 20 in the third region III may be defined as a third insulating layer 113.

[0076] Referring to FIG. 18, a gate spacer may be formed on both side walls of the plurality of dummy gates DG in the first horizontal direction DR1. For example, a first gate spacer 121 may be formed on both side walls of the dummy gate DG in the first region I, a second gate spacer 122 may be formed on both side walls of the dummy gate DG in the second region II, and a third gate spacer 123 may be formed on both side walls of the dummy gate DG in the third region III.

[0077] The first gate spacer 121 may also be formed on side walls of the sixth mask pattern M6 in the first region I. The second gate spacer 122 may also be formed on each of side walls of the sixth mask pattern M6 in the second region II and side walls of the second insulating layer 112 in the second region II. The third gate spacer 123 may also be formed on side walls of the sixth mask pattern M6 in the third region III, side walls of the second insulating layer 112 in the third region III, and side walls of the third insulating layer 113 in the third region III.

[0078] Subsequently, a third protective layer 60 may be formed in the first and third regions I and III. Subsequently, a part of the first active pattern F1 may be etched, using the dummy gate DG and the first gate spacer 121 in the first region I as masks. Subsequently, the

first source/drain region SD1 may be formed in the portion in which a part of the first active pattern F1 is etched.

[0079] Referring to FIG. 19, the third protective layer 60 may be removed.

Subsequently, a first interlayer insulating layer 140 may be formed on the first to third gate spacers 121, 122 and 123, the first to third source/drain regions SD1, SD2 and SD3, and the sixth mask pattern M6. Subsequently, a part of the first interlayer insulating layer 140 and the sixth mask pattern M6 may be etched through a flattening process to expose a plurality of dummy gates DG.

[0080] After that, the plurality of dummy gates DG may be removed to form first to third gate trenches GT1, GT2, and GT3. According to an embodiment, the first gate trench GT1 may be defined by the first gate spacer 121 on the first active pattern F1 in the first region I. The second gate trench GT2 may be defined by the second gate spacer 122 on the second insulating layer 112 in the second region II. The third gate trench GT3 may be defined by the third gate spacer 123 on the second insulating layer 112 in the third region III.

[0081] Referring to FIG. 20, a first insulating layer 111 may be formed on each of the first active pattern F1, the second insulating layer 112 on the second active region AR2, and the second insulating layer 112 on the third active region AR3.

[0082] For example, the first insulating layer 111 may be formed along side walls and a bottom surface of the first gate trench (GT1 of FIG. 19) in the first region I. The first insulating layer 111 may be formed along side walls and a bottom surface of the second gate trench (GT2 of FIG. 19) in the second region II. The first insulating layer 111 may be formed along side walls and a bottom surface of the third gate trench (GT3 of FIG. 19) in the third region III.

[0083] Subsequently, a gate electrode may be formed on the first insulating layer 111.

For example, a first gate electrode G1 may be formed on the first insulating layer 111 in the first region I. A second gate electrode G2 may be formed on the first insulating layer 111 in the second region II. A third gate electrode G3 may be formed on the first insulating layer 111 in the third region III. Each of the first to third gate electrodes G1, G2, and G3 may extend in the second horizontal direction DR2.

[0084] Subsequently, a first capping pattern 131 may be formed on the first gate electrode G1, the first insulating layer 111, and the first gate spacer 121. A second capping pattern 132 may be formed on the second gate electrode G2, the first insulating layer 111, and the second gate spacer 122. A third capping pattern 133 may be formed on the third gate electrode G3, the first insulating layer 111, and the third gate spacer 123.

[0085] Thicknesses of each of the first to third gate electrodes G1, G2, and G3 in the vertical direction DR3 may be formed to be equal to one another. For example, a first thickness (t_1 of FIG. 2) in the vertical direction DR3 of the first gate electrode G1 that overlaps the first active pattern F1 in the vertical direction DR3, a second thickness (t_2 of FIG. 2) in the vertical direction DR3 of the second gate electrode G2 that overlaps the second active region AR2 in the vertical direction DR3, and a third thickness (t_3 of FIG. 2) in the vertical direction DR3 of the third gate electrode G3 that overlaps the third active region AR3 in the vertical direction DR3 may be formed to be equal to one another.

[0086] The upper surfaces of each of the first to third gate electrodes G1, G2, and G3 may be formed at a same level on the substrate 100. For example, an upper surface G1u of the first gate electrode G1 that is in contact with the lowermost surface of the first capping pattern 131, an upper surface G2u of the second gate electrode G2 that is in contact with the lowermost surface of the second capping pattern 132, and an upper surface G3u of the third gate electrode G3 that is in contact with the lowermost surface of the third capping pattern

133 may be formed at a same level on the substrate 100.

[0087] Subsequently, an etching stop layer 150 and a second interlayer insulating layer 160 may be sequentially formed on the first interlayer insulating layer 140 and each of the first to third capping patterns 131, 132 and 133, as shown in FIG. 2.

[0088] The semiconductor device and the method for manufacturing a semiconductor device according to the above embodiments may enable a low voltage transistor, an intermediate voltage transistor, and a high voltage transistor formed on a same substrate to have respective gate electrodes having a same thickness and respective gate insulating layers having different thicknesses, thereby to be formed at a same level on the substrate.

[0089] Hereinafter, a method for manufacturing a semiconductor device according to other embodiments will be described referring to FIGS. 21 to 27. Differences from the method for manufacturing the semiconductor device shown in FIGS. 3 to 20 will be described herebelow, and duplicate descriptions will be omitted.

[0090] FIGS. 21 to 27 are intermediate stage diagrams for explaining a method for manufacturing a semiconductor device according to other embodiments.

[0091] Referring to FIG. 21, a substrate 100 is provided in which first to third regions I, II and III are defined. Subsequently, a first mask pattern M1 may be formed on an upper surface of the substrate 100. Subsequently, the upper surface of the substrate 100 at the second region II may be etched using the first mask pattern M1 as a mask to form a first trench TR1. Further, the upper surface of the substrate 100 at the third region III may be etched using the first mask pattern M1 as a mask to form a third trench TR3. The third trench TR3 may be formed to be deeper than the first trench TR1. That is, a lower surface of the third trench TR3 may be formed at a level lower than a lower surface of the first trench TR1.

[0092] Referring to FIG. 22, a first insulating material layer 10 may be formed inside

each of the first trench TR1 and the third trench TR3. After that, the first mask pattern M1 may be removed through a flattening process.

[0093] Referring to FIG. 23, a second mask pattern M2 may be formed on the upper surface of the substrate 100 and the first insulating material layer 10. Subsequently, a part of the substrate 100 at the first region I may be etched using the second mask pattern M2 as a mask to form first and second active patterns F1 and F2 extending in the first horizontal direction DR1.

[0094] Referring to FIG. 24, a field insulating layer 105 may be formed to surround side walls of each of the first and second active patterns F1 and F2 and side walls of the second mask pattern M2. For example, an upper surface of the field insulating layer 105 may be formed on a same plane as an upper surface of the second mask pattern M2.

[0095] Referring to FIG. 25, a third mask pattern M3 may be formed on the field insulating layer 105 and the second mask pattern M2. Subsequently, a part of the second mask pattern M2, a part of the first insulating material layer 10, a part of the field insulating layer 105, and a part of the substrate 100 may be etched, using the third mask pattern M3 as a mask. Through this etching process, a first deep trench DT1 may be formed on the substrate 100 at the first region I, a second deep trench DT2 is formed on the substrate 100 at the second region II, and a third deep trench DT3 may be formed on the substrate 100 at the third region III.

[0096] Referring to FIG. 26, the field insulating layer 105 may also be formed inside each of the first to third deep trenches DT1, DT2, and DT3. Subsequently, the third mask pattern M3 and the second mask pattern M2 may be removed through a flattening process.

[0097] Referring to FIG. 27, a fourth mask pattern M4 may be formed in the first region I and the second region II. Subsequently, a part of the field insulating layer 105 and a

part of the first insulating material layer 10 formed in the third region III may be etched, using the fourth mask pattern M4 as a mask. The remaining unetched first insulating material layer 10 in the third region III may be defined as the second insulating material layer 20. For example, an upper surface of the second insulating material layer 20 in the third region III may be formed at a same level as an upper surface of the second active region AR2 in the second region II.

[0098] Subsequently, after performing the manufacturing processes shown in FIGS. 11 to 20, an etching stop layer 150 and a second interlayer insulating layer 160 may be sequentially formed on the first interlayer insulating layer 140 and each of first to third capping patterns 131, 132 and 133. The semiconductor device shown in FIG. 2 may be manufactured through the foregoing method.

[0099] Hereinafter, a semiconductor device according to other embodiments will be described referring to FIG. 28. Differences from the semiconductor device shown in FIGS. 1 and 2 will be described herebelow, and duplicate descriptions will be omitted.

[0100] FIG. 28 is a cross-sectional view for explaining a semiconductor device, according to other embodiments.

[0101] Referring to FIG. 28, in a semiconductor device according to other embodiments, a first insulating layer 211 may be formed on a bottom surfaces of each of first to third gate electrodes G21, G22, and G23. According to an embodiment, side walls of the first gate electrode G21 may be in contact with the first gate spacer 221. Side walls of the second gate electrode G22 may be in contact with a second gate spacer 222. Side walls of the third gate electrode G23 may be in contact with a third gate spacer 223.

[0102] A first capping pattern 231 may be disposed on the first gate electrode G21, a second capping pattern 232 may be disposed on the second gate electrode G22, and a third

capping pattern 233 may be disposed on the third gate electrode G23. The first capping pattern 231 is disposed between the first gate spacers 221, the second capping pattern 232 is disposed between the second gate spacers 222, and the third capping patterns 233 may be disposed between the third gate spacers 223.

[0103] Thicknesses of the first to third gate electrodes G21, G22, and G23 in the vertical direction DR3 may be equal to one another. For example, a fourth thickness t_4 in the vertical direction DR3 of the first gate electrode G21 that overlaps a first active pattern F1 in the vertical direction DR3, a fifth thickness t_5 in the vertical direction DR3 of the second gate electrode G22 that overlaps a second active region AR2 in the vertical direction DR3, and a sixth thickness t_6 in the vertical direction DR3 of the third gate electrode G23 that overlaps a third active region AR3 in the vertical direction DR3 may be equal to one another.

[0104] Upper surfaces of the first to third gate electrodes G21, G22, and G23 may be formed at a same level on a substrate 100. For example, an upper surface G21u of the first gate electrode G21 that is in contact with the lowermost surface of the first capping pattern 231, an upper surface G22u of the second gate electrode G22 that is in contact with the lowermost surface of the second capping pattern 232, and an upper surface G23u of the third gate electrode G23 that is in contact with the lowermost surface of the third capping pattern 233 may be formed at a same level on the substrate 100.

[0105] Hereinafter, a method for manufacturing a semiconductor device according to other embodiments will be described referring to FIGS. 28 to 32. Differences from the method for fabricating the semiconductor device shown in FIGS. 3 to 20 will be described, and duplicate descriptions will be omitted.

[0106] FIGS. 29 to 32 are intermediate stage diagrams for explaining a method for manufacturing a semiconductor device, according to other embodiments.

[0107] Referring to FIG. 29, after performing the manufacturing processes shown in FIGS. 3 to 15, a second protective layer (50 of FIG. 15) and a fifth mask pattern (M5 of FIG. 15) in second and third regions II and III may be removed. Subsequently, a fourth insulating material layer 80 may be formed on first and second active patterns F1 and F2 in a first region I, a field insulating layer 105 in the first region I, and a third insulating material layer 40 in the second and third regions II and III. For example, the fourth insulating material layer 80 may be conformally formed.

[0108] Subsequently, a gate material layer GM may be formed on the fourth insulating material layer 80 in the first to third regions I, II and III. Upper surface of the gate material layer GM may be formed flat through a flattening process. Next, a capping material layer 130M may be formed on the gate material layer GM in the first to third regions I, II and III. For example, the capping material layer 130M may be conformally formed.

[0109] Referring to FIG. 30, through a patterning process, the fourth insulating material layer 80 is etched to form a first insulating layer 211, and the gate material layer GM may be etched to form first to third gate electrodes G21, G22 and G23.

[0110] Specifically, a sixth mask pattern M6 may be formed on the capping material layer 130M. Next, the capping material layer 130M, the gate material layer GM, the fourth insulating material layer 80, the third insulating material layer 40, and a second insulating material layer 20 may be etched using the sixth mask pattern M6 as a mask.

[0111] For example, in the first region I, by utilizing the sixth mask pattern M6 as a mask, the capping material layer 130M may be etched to form a first capping pattern 231, the gate material layer GM may be etched to form the first gate electrode G21, and the fourth insulating material layer 80 may be etched to form the first insulating layer 211.

[0112] Further, in the second region II, by utilizing the sixth mask pattern M6 as a

mask, the capping material layer 130M may be etched to form a second capping pattern 232, the gate material layer GM may be etched to form the second gate electrode G22, the fourth insulating material layer 80 may be etched to form the first insulating layer 211, and the third insulating material layer 40 may be etched to form a second insulating layer 112.

[0113] Further, in the third region III, by utilizing the sixth mask pattern M6 as a mask, the capping material layer 130M may be etched to form a third capping pattern 233, the gate material layer GM may be etched to form the third gate electrode G23, the fourth insulating material layer 80 may be etched to form the first insulating layer 211, the third insulating material layer 40 may be etched to form the second insulating layer 112, and the second insulating material layer 20 may be etched to form a third insulating layer 113.

[0114] Referring to FIG. 31, the sixth mask pattern M6 may be removed. Subsequently, in the first region I, a first gate spacer 221 may be formed on both side walls of each of the first capping pattern 231, the first gate electrode G21 and the first insulating layer 211 in the first horizontal direction DR1.

[0115] Further, in the second region II, a second gate spacer 222 may be formed on both side walls of each of the second capping pattern 232, the second gate electrode G22, the first insulating layer 211, and the second insulating layer 112 in the first horizontal direction DR1. Further, in the third region III, a third gate spacer 223 may be formed on both side walls of each of the third capping pattern 233, the third gate electrode G23, the first insulating layer 211, the second insulating layer 112, and the third insulating layer 113 in the first horizontal direction DR1.

[0116] Referring to FIG. 32, a third protective layer 60 may be formed in the first and third regions I and III. Subsequently, a part of the first active pattern F1 may be etched, using the first capping pattern 231 and the first gate spacer 221 in the first region I as masks.

Subsequently, a first source/drain region SD1 may be formed where a part of the first active pattern F1 is etched.

[0117] Referring to FIG. 28, the third protective layer 60 may be removed.

Subsequently, the first to third gate spacers 221 and 222, 223, the first to third source/drain regions SD1, SD2 and SD3, and the first interlayer insulating layer 140 may be formed.

Subsequently, a part of the first interlayer insulating layer 140 may be etched through a flattening process to expose the first to third capping patterns 231, 232 and 233.

[0118] Subsequently, the etching stop layer 150 and the second interlayer insulating layer 160 may be sequentially formed on the first interlayer insulating layer 140 and each of the first to third capping patterns 231, 232, and 233. The semiconductor device shown in FIG. 28 may be manufactured through the foregoing method.

[0119] Hereinafter, a semiconductor device according to other embodiments will be described referring to FIG. 33. Differences from the semiconductor device shown in FIGS. 1 and 2 will be described, and duplicate descriptions will be omitted.

[0120] FIG. 33 is a cross-sectional view for explaining a semiconductor device according to some other embodiments.

[0121] Referring to FIG. 33, in a semiconductor device according to other embodiments, a first insulating layer 111 may be disposed along side walls and a bottom surface of a first gate electrode G1 in the first region I. Further, a first insulating layer 211 may be formed on a bottom surface of a second gate electrode G22 in the second region II. Further, a first insulating layer 211 may be formed on a bottom surface of a third gate electrode G23 in the third region III. According to an embodiment, side walls of the second gate electrode G22 may be in contact with the second gate spacer 222, and side walls of the third gate electrode G23 may be in contact with a third gate spacer 223.

[0122] A second capping pattern 232 may be disposed on the second gate electrode G22, and a third capping pattern 233 may be disposed on the third gate electrode G23. The second capping pattern 232 may be disposed between the second gate spacers 222, and the third capping pattern 233 may be disposed between the third gate spacers 223.

[0123] Thicknesses of the first to third gate electrodes G1, G22, and G23 in the vertical direction DR3 may be equal to one another. For example, a first thickness t1 in the vertical direction DR3 of the first gate electrode G1 that overlaps a first active pattern F1 in the vertical direction DR3, a fifth thickness t5 in the vertical direction DR3 of the second gate electrode G22 that overlaps a second active region AR2 in the vertical direction DR3, and a sixth thickness t6 in the vertical direction DR3 of the third gate electrode G23 that overlaps a third active region AR3 in the vertical direction DR3 may be equal to one another.

[0124] Upper surfaces of the first to third gate electrodes G1, G22, and G23 may be formed at a same level on a substrate 100. For example, an upper surface G1u of the first gate electrode G1 that is in contact with a bottom surface of a first capping pattern 131, an upper surface G22u of the second gate electrode G22 that is in contact with a bottom surface of a second capping pattern 232, and an upper surface G23u of the third gate electrode G23 that is in contact with a bottom surface of a third capping pattern 233 may be formed at a same level on a substrate 100.

[0125] In concluding the detailed description, those skilled in the art will appreciate that many variations and modifications may be made to the above embodiments without substantially departing from the principles. Therefore, the embodiments of the disclosure are used in a generic and descriptive sense only and not for purposes of limitation.

CLAIMS

1. A semiconductor device comprising:
 - a substrate comprising first and second regions thereon;
 - a first active region in the first region;
 - an active pattern on the first active region;
 - a second active region in the second region;
 - a first gate electrode on the active pattern;
 - a second gate electrode on the second active region;
 - a first gate insulating layer, comprising a first-first insulating layer, between the active pattern and the first gate electrode; and
 - a second gate insulating layer, comprising a second-first insulating layer and a second-second insulating layer below the second-first insulating layer, between the second active region and the second gate electrode,

wherein a thickness in a vertical direction of the first gate electrode that overlaps the active pattern in the vertical direction is equal to a thickness in the vertical direction of the second gate electrode that overlaps the second active region in the vertical direction, and

wherein an upper surface of the first gate electrode is formed at a same level as an upper surface of the second gate electrode.
2. The semiconductor device of claim 1, wherein an upper surface of the second active region is at a level between an upper surface of the first active region and an upper surface of the active pattern.
3. The semiconductor device of claim 1 or claim 2, wherein the first-first insulating layer is on side walls and a bottom surface of the first gate electrode.

4. The semiconductor device of any one of claims 1 to 3, wherein the second-first insulating layer is on side walls and a bottom surface of the second gate electrode.

5. The semiconductor device of claim 1 or claim 2, further comprising:
a first gate spacer on side walls of the first gate electrode; and
a second gate spacer on side walls of the second gate electrode,
wherein the first-first gate insulating layer is between the first gate spacers, and the second-first gate insulating layer is between the second gate spacers.

6. The semiconductor device of claim 5, wherein the side walls of the first gate electrode are in contact with the first gate spacer, and
wherein the side walls of the second gate electrode are in contact with the second gate spacer.

7. The semiconductor device of any one of claims 1 to 6, further comprising:
a third region on the substrate;
a third active region in the third region;
a third gate electrode in the third active region; and
a third gate insulating layer, comprising a third-first insulating layer, a third-second insulating layer below the third-first insulating layer, and a third-third insulating layer below the third-second insulating layer, between the third active region and the third gate electrode.

8. The semiconductor device of claim 7, wherein a thickness in the vertical direction of the third gate electrode that overlaps the third active region in the vertical

direction is equal to the thickness in the vertical direction of the first gate electrode that overlaps the active pattern in the vertical direction.

9. The semiconductor device of claim 7 or claim 8, wherein an upper surface of the third gate electrode is formed at a same level as the upper surface of the first gate electrode.

10. A semiconductor device comprising:

- a substrate comprising first to third regions thereon;
- a first active region in the first region;
- an active pattern on the first active region;
- a second active region in the second region;
- a third active region in the third region;
- a first gate electrode on the active pattern;
- a second gate electrode on the second active region;
- a third gate electrode on the third active region;
- a first gate insulating layer, comprising a first-first insulating layer, between the active pattern and the first gate electrode; and
- a second gate insulating layer, comprising a second-first insulating layer and a second-second insulating layer below the second-first insulating layer, between the second active region and the second gate electrode; and
- a third gate insulating layer, comprising a third-first insulating layer, a third-second insulating layer below the third-first insulating layer, and a third-third insulating layer below the third-second insulating layer, between the third active region and the third gate electrode,

wherein a thickness in a vertical direction of the first gate electrode that overlaps the

active pattern in the vertical direction, a thickness in the vertical direction of the second gate electrode that overlaps the second active region in the vertical direction, and a thickness in the vertical direction of the third gate electrode that overlaps the third active region in the vertical direction are equal to one another, and

wherein an upper surface of the first gate electrode, an upper surface of the second gate electrode, and an upper surface of the third gate electrode are formed at a same level on the substrate.

11. The semiconductor device of claim 10, wherein a thickness of the third-third insulating layer in the vertical direction is greater than a thickness of the third-second insulating layer in the vertical direction, and

wherein the thickness of the third-second insulating layer in the vertical direction is greater than a thickness of the third-first insulating layer.

12. The semiconductor device of claim 10 or claim 11, wherein an upper surface of the second active region is formed at a level lower than an upper surface of the active pattern, and

wherein an upper surface of the third active region is formed at a level lower than the upper surface of the second active region.

13. The semiconductor device of any one of claims 10 to 12, further comprising:
a first source/drain region disposed on at least one side of the first gate electrode;
a second source/drain region disposed on at least one side of the second gate electrode; and

a third source/drain region disposed on at least one side of the third gate electrode,

wherein an upper surface of the second source/drain region is formed at a level lower than an upper surface of the first source/drain region, and

wherein an upper surface of the third source/drain region is formed at a level lower than the upper surface of the second source/drain region.

14. The semiconductor device of claim 13, wherein a thickness of the third source/drain region in the vertical direction is greater than a thickness of the second source/drain region in the vertical direction.

15. A method for manufacturing a semiconductor device, the method comprising:
providing a substrate comprising first to third regions thereon;
etching an upper surface of the substrate at the second region to form a first trench,
and etching the upper surface of the substrate at the third region to form a second trench;
forming a first insulating material layer inside each of the first and second trenches;
etching the substrate at the first region to form an active pattern;
etching the substrate at each of the first to third regions to form first to third active regions;
etching at least a part of the first insulating material layer formed on the third active region;
forming a second insulating material layer on the third active region;
etching the first insulating material layer formed on the second active region;
forming a third insulating material layer on each of the second active region and the second insulating material layer of the third active region;
forming an insulating layer on each of the active pattern, the third insulating material layer formed on the second active region, and the third insulating material layer formed on

the third active region; and

forming a first gate electrode on the insulating layer on the active pattern, forming a second gate electrode on the insulating layer on the second active region, and forming a third gate electrode on the insulating layer on the third active region,

wherein a thickness in a vertical direction of the first gate electrode that overlaps the active pattern in the vertical direction, a thickness in the vertical direction of the second gate electrode that overlaps the second active region in the vertical direction, and a thickness in the vertical direction of the third gate electrode that overlaps the third active region in the vertical direction are equal to one another, and

wherein an upper surface of the first gate electrode, an upper surface of the second gate electrode, and an upper surface of the third gate electrode are formed at a same level.

16. The method for fabricating the semiconductor device of claim 15, wherein the formation of the second insulating material layer on the third active region comprises:

completely etching the first insulating material layer formed on the third active region; and

oxidizing a part of an upper part of the third active region to form the second insulating material layer.

17. The method for fabricating the semiconductor device of claim 15, wherein the formation of the second insulating material layer on the third active region comprises etching a part of the first insulating material layer formed on the third active region to form the second insulating material layer on the third active region.

18. The method for fabricating the semiconductor device of claim 17, wherein a

lower surface of the second trench is formed at a level lower than a lower surface of the first trench.

19. The method for fabricating the semiconductor device of any one of claims 15 to 18, wherein the formation of the insulating layer comprises:

forming a dummy gate on each of the active pattern, the third insulating material layer formed on the second active region, and the third insulating material layer formed on the third active region;

forming a gate spacer on side walls of the dummy gate;

removing the dummy gate to form a gate trench; and

forming the insulating layer on side walls and a bottom surface of the gate trench.

20. The method for fabricating the semiconductor device of any one of claims 15 to 18, wherein the formation of the insulating layer and the first to third gate electrodes comprises:

forming a fourth insulating material layer on each of the active pattern, the third insulating material layer formed on the second active region, and the third insulating material layer formed on the third active region;

forming a gate material layer on the fourth insulating material layer; and

patterning the fourth insulating material layer and the gate material layer to form the insulating layer and the first to third gate electrodes.