AN SRAM CELL STRUCTURE AND METHOD OF MANUFACTURE THEREOF

ABSTRACT OF THE DISCLOSURE

An SRAM transistor cell on a doped semiconductor substrate comprises two access FET transistors and two storage FET transistors. A first load capacitor has a plate connected to a first node with the other plate connected to the power supply. A second load capacitor has a plate connected to the second node with the other plate connected to the power supply, a bit line and a bit line bar. The first storage transistor drain connects to the first node. The second storage transistor drain connects to the second node. The storage transistors have interconnected sources. The first node connects via a first interconnection line to the second transistor gate. The second node connects via a second interconnection line to the first transistor gate. First and second access transistor gates connect to a wordline. The first access transistor drain connects to the first node. The second access transistor drain connects to the second node. The first access transistor source connects to the bit line. The second access transistor source connects to the bit line bar.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)