FIG. 1

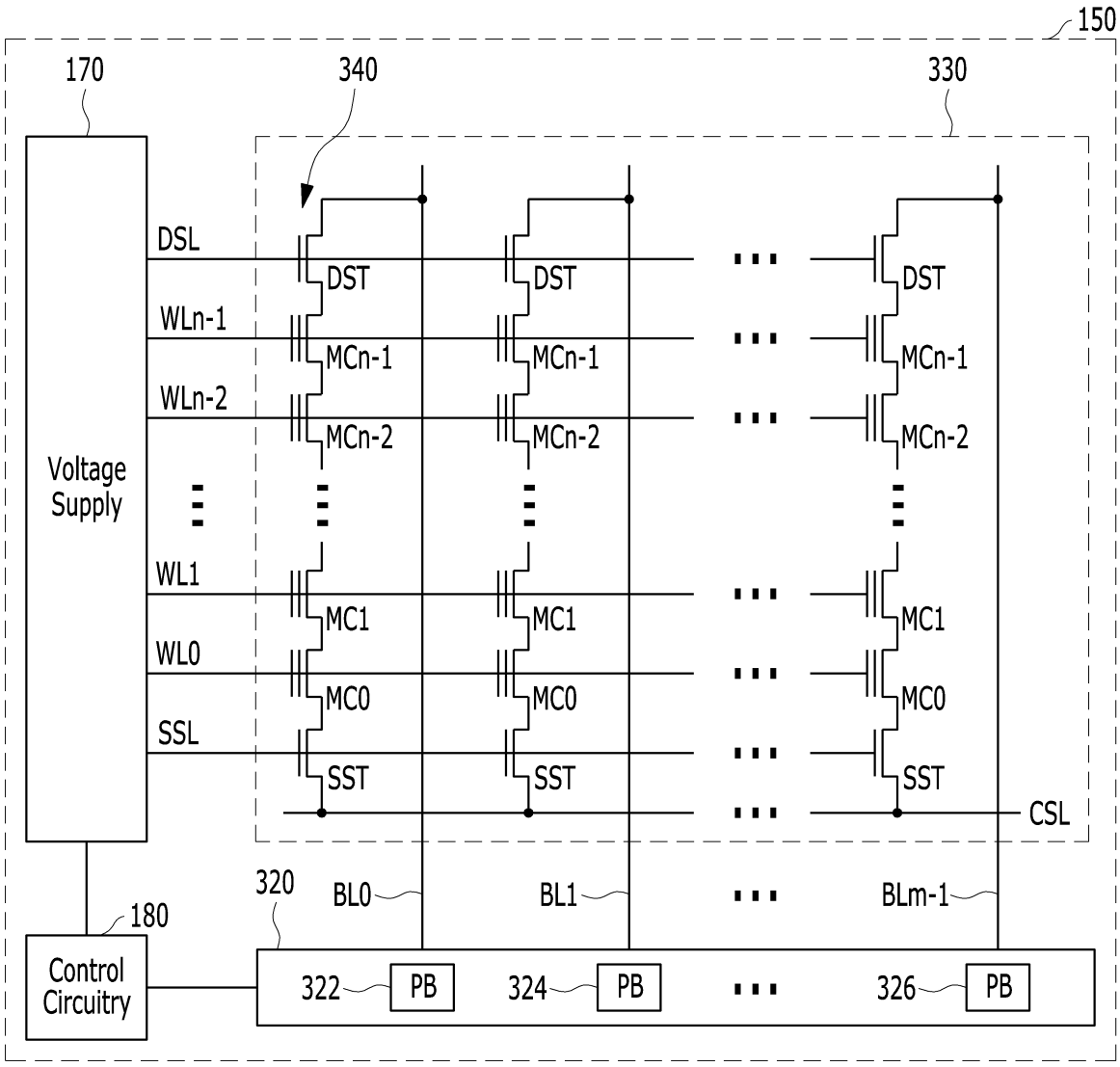

150
170
340
330
Voltage Supply
DSL
WLn-1
WLn-2
WL1
WL0
SSL
DST
MCn-1
MCn-2
MC1
MC0
SST
CSL
320
BL0
BL1
BLm-1
180
Control Circuitry
322
PB
324
PB
326
PB

FIG. 2

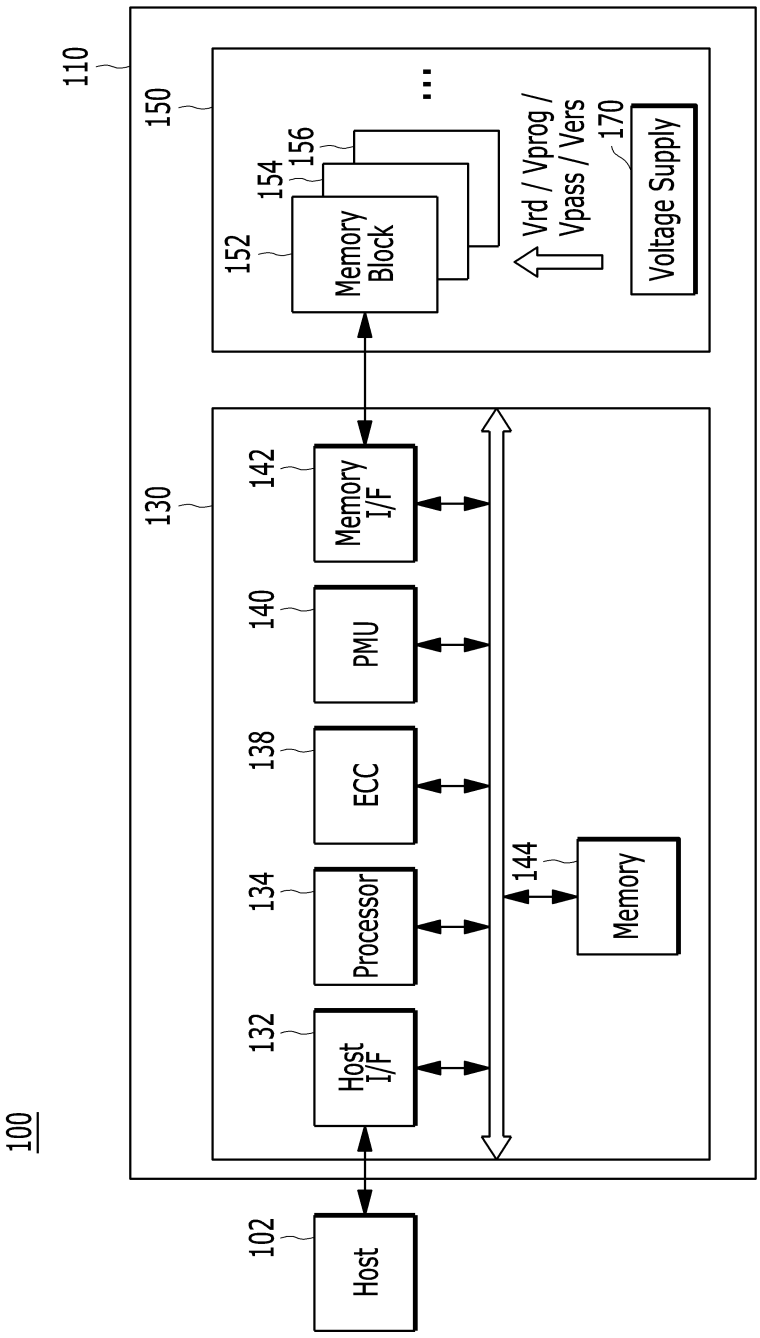

100
110
150
152
Memory Block
154
156
...
Vrd / Vprog / Vpass / Vers
170
Voltage Supply
130
142
Memory I/F
140
PMU
138
ECC
134
Processor
144
Memory
132
Host I/F
102
Host

FIG. 3

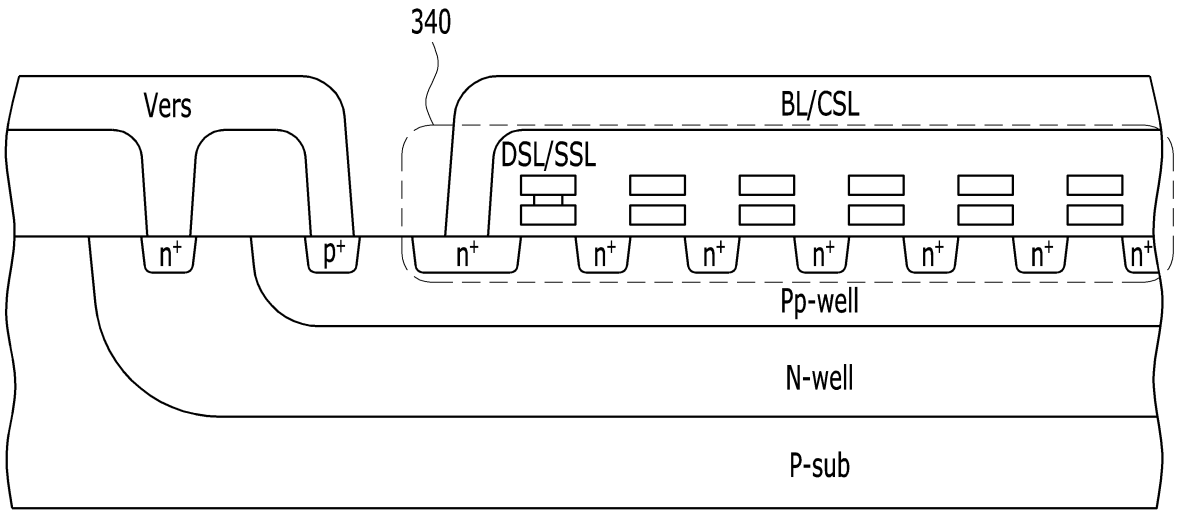


FIG. 4

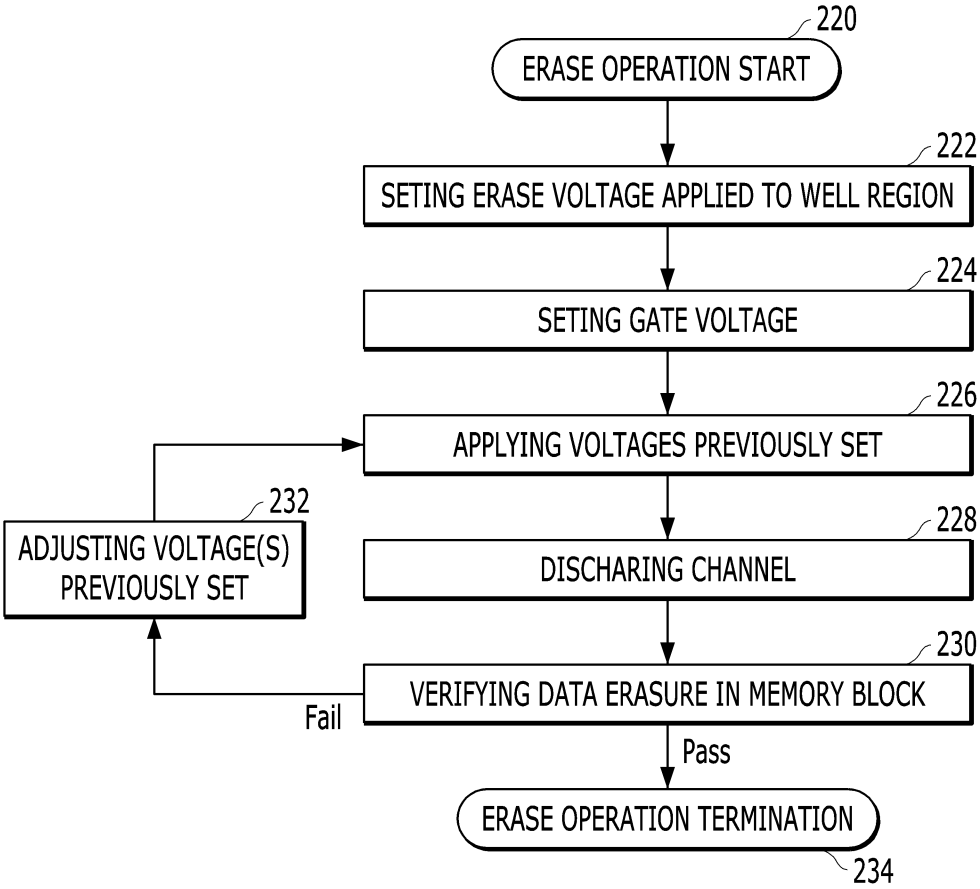

220
ERASE OPERATION START
222
SETING ERASE VOLTAGE APPLIED TO WELL REGION
224
SETING GATE VOLTAGE
226
APPLYING VOLTAGES PREVIOUSLY SET
228
DISCHARING CHANNEL
230
VERIFYING DATA ERASURE IN MEMORY BLOCK
Fail
232
ADJUSTING VOLTAGE(S) PREVIOUSLY SET
Pass
ERASE OPERATION TERMINATION
234

FIG. 5

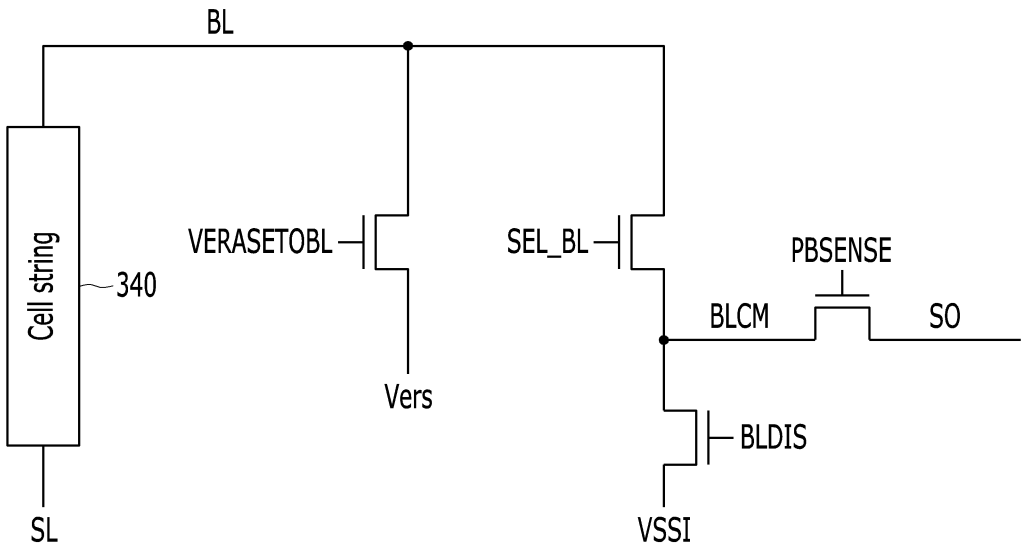

BL
Cell string
340
SL
VERASETOBL
Vers
SEL_BL
PBSENSE
BLCM
SO
BLDIS
VSSI

FIG. 6

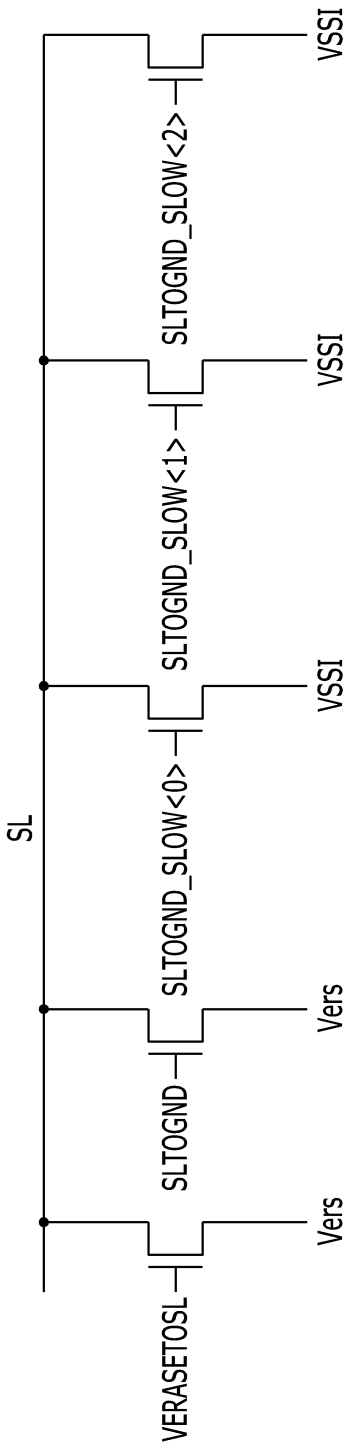

SL
VERASETOSL
SLTOGND
SLTOGND_SLOW<0>
SLTOGND_SLOW<1>
SLTOGND_SLOW<2>
Vers
Vers
VSSI
VSSI
VSSI

FIG. 7

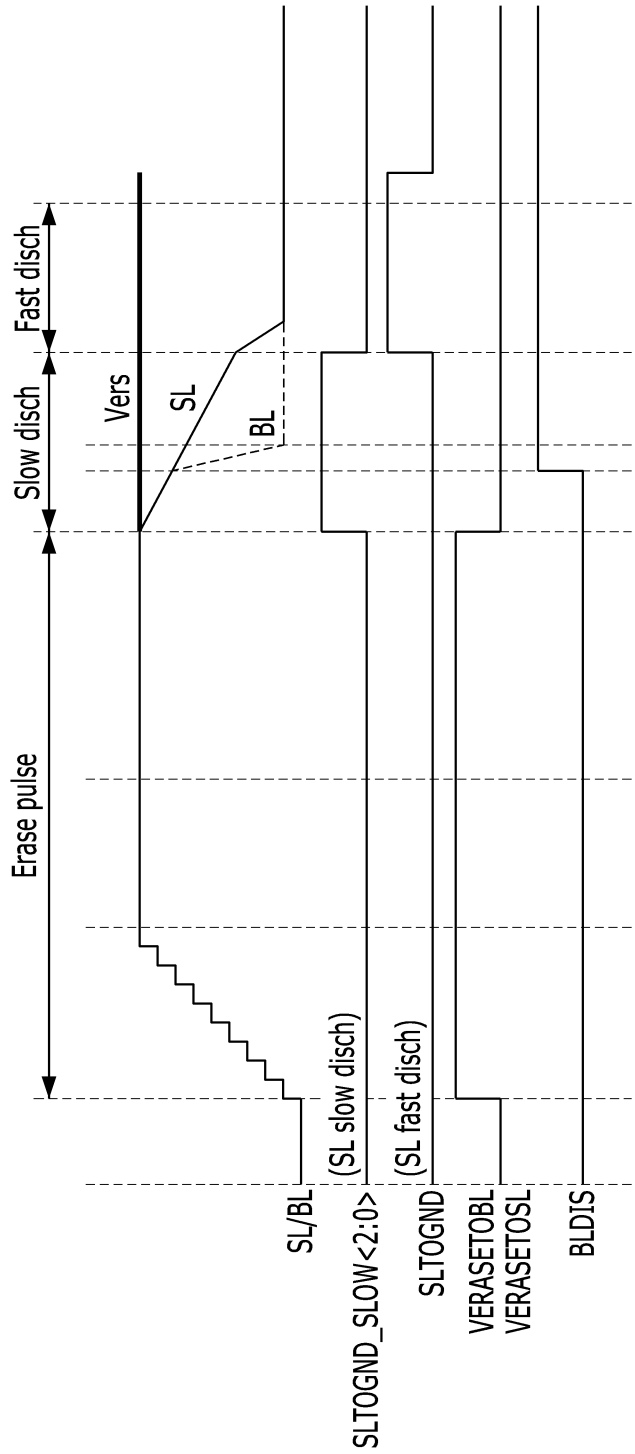

Fast disch
Slow disch
Erase pulse
Vers
SL
BL
SL/BL
SLTOGND_SLOW<2:0>
(SL slow disch)
(SL fast disch)
SLTOGND
VERASETOBL
VERASETOSL
BLDIS

FIG. 8

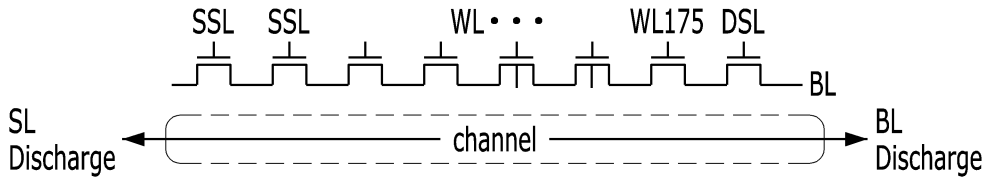

SSL
SSL
WL • • •
WL175
DSL
BL
SL
Discharge
channel
BL
Discharge

FIG. 9

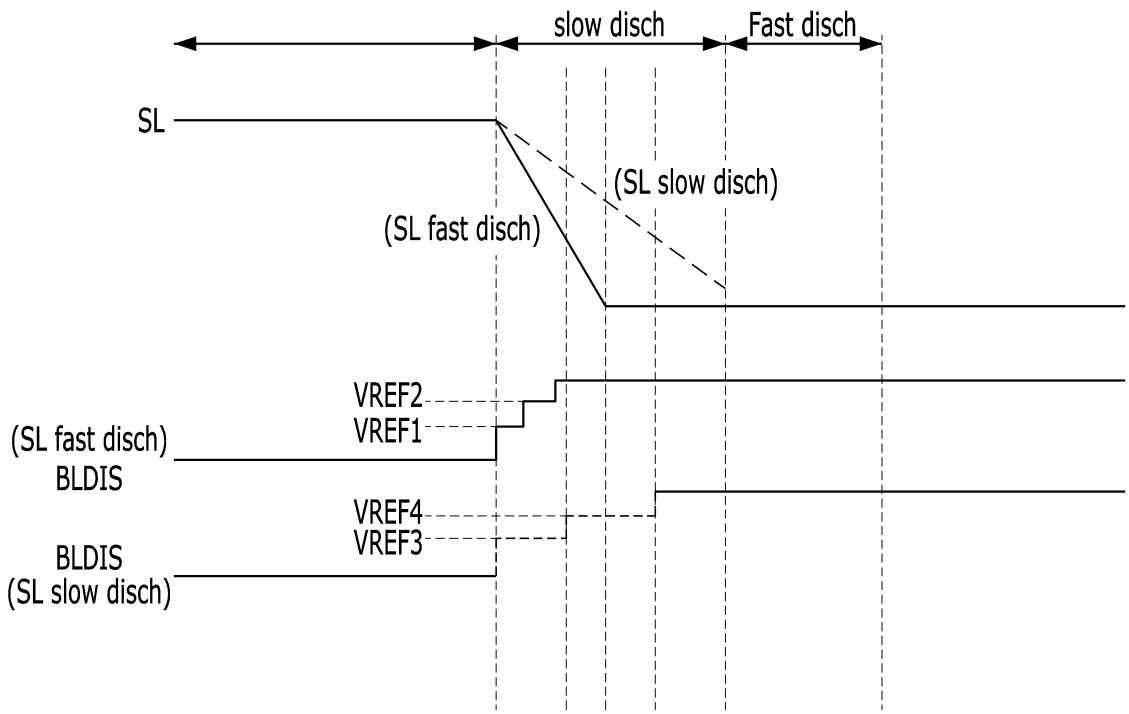

slow disch
Fast disch
SL
(SL slow disch)
(SL fast disch)
VREF2
VREF1
(SL fast disch)
BLDIS
VREF4
VREF3
BLDIS
(SL slow disch)

FIG. 10

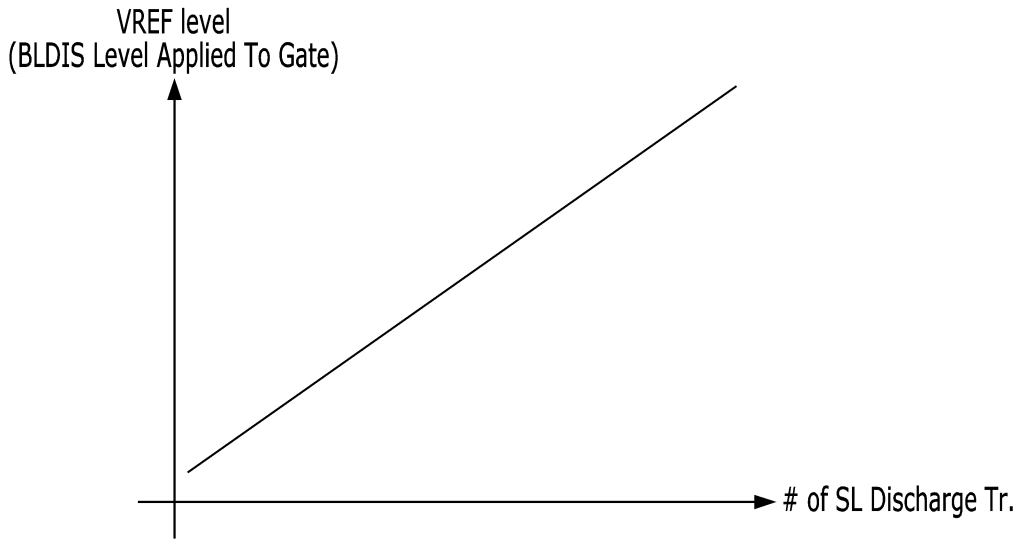

VREF level
(BLDIS Level Applied To Gate)
# of SL Discharge Tr.

FIG. 11

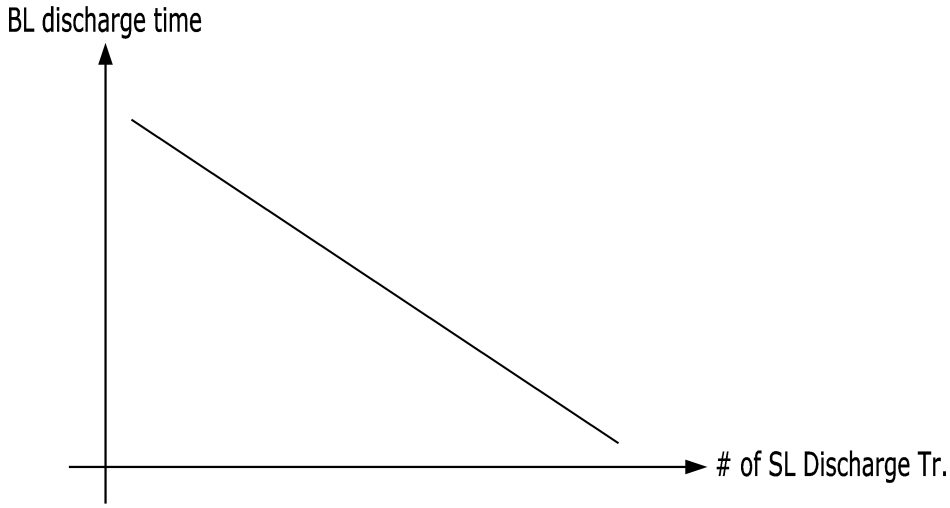

BL discharge time
# of SL Discharge Tr.

FIG. 12

