DESCRIPTION

STORAGE DEVICE

FIELD

Embodiments described herein relate generally to a storage device.

BACKGROUND

In storage devices, in order to improve the package density, multiple memory chips are stacked on a control chip. In this case, it is desired to reduce the consumption current of the storage device.

~~CITATION LIST~~

~~PATENT LITERATURE~~

~~[PTL 1] Japanese Patent Application Laid-open No. 2011-81730~~

~~[PTL 2] Japanese Patent Application Laid-open No. 2011-81884~~

~~SUMMARY~~

~~TECHNICAL PROBLEM~~

~~An object of one embodiment is to provide a storage device which can reduce the consumption current.~~

~~SOLUTION TO PROBLEM~~

~~In general, according to one embodiment, there is provided a storage device including a control chip and a plurality of memory chips. The control chip has an input buffer common to the control chip and the plurality of memory chips and electrically connected to an external terminal. A first transmission path going through the input buffer and a second transmission path not going~~

~~through the input buffer are provided between the external terminal and the plurality of memory chips. In a first mode, the control chip enables the input buffer so as to activate the first transmission path and, in a second mode, disables the input buffer so as to activate the second transmission path.~~

BRIEF DESCRIPTION OF THE DRAWINGS

~~FIG. 1~~ is a~~A~~ cross-sectional view showing the configuration of a storage device according to a first embodiment.

~~FIG. 2~~ is a~~A~~ circuit diagram showing the input terminal related configuration of the storage device according to the first embodiment.

~~FIG. 3~~ is a~~A~~ cross-sectional view showing the configuration of a storage device according to a modified example of the first embodiment.

~~FIG. 4~~ is a~~A~~ circuit diagram showing the input terminal related configuration of the storage device according to the modified example of the first embodiment.

~~FIG. 5~~ is a~~A~~ circuit diagram showing the input terminal related configuration of a storage device according to a second embodiment.

~~FIG. 6~~ is a~~A~~ circuit diagram showing the input terminal related configuration of a storage device according to a third embodiment.

~~FIG. 7~~ is a~~A~~ circuit diagram showing the input terminal related configuration of a storage device according to a fourth embodiment.

~~FIG. 8~~ is a~~A~~ circuit diagram showing the output terminal related configuration of a storage device according to a fifth embodiment.

~~FIG. 9~~ is a~~A~~ circuit diagram showing the output

terminal related configuration of a storage device according to a sixth embodiment.

~~FIG. 10~~ is a~~A~~ circuit diagram showing the output terminal related configuration of a storage device according to a seventh embodiment.

~~FIG. 11~~ is a~~A~~ circuit diagram showing the input terminal related configuration of a storage device in basic form.

~~FIG. 12~~ is a~~A~~ circuit diagram showing the output terminal related configuration of the storage device in basic form.

DETAILED DESCRIPTION

In general, according to one embodiment, there is provided a storage device including a control chip and a plurality of memory chips. The control chip has an input buffer common to the control chip and the plurality of memory chips and electrically connected to an external terminal. A first transmission path going through the input buffer and a second transmission path not going through the input buffer are provided between the external terminal and the plurality of memory chips. In a first mode, the control chip enables the input buffer so as to activate the first transmission path and, in a second mode, disables the input buffer so as to activate the second transmission path.

Exemplary embodiments of a storage device will be explained below in detail with reference to the accompanying drawings. The present invention is not limited to the following embodiments.

(First Embodiment)

A storage device 100 according to the first embodiment will be described using FIG. 1. FIG. 1 is a cross-

sectional view showing the configuration of the storage device 100.

In the storage device 100, in order to improve the package density, multiple memory chips 10 are stacked on a control chip 20. For example, in the storage device 100, the control chip 20, a memory chip 10-1, and a memory chip 10-2 are stacked in that order on a basal plate 1 as shown in FIG. 1. They are encapsulated by encapsulation resin 30 filling spaces around them. In this case, for example, external terminals 2 are connected with elements in the chips with use of TSVs (Through Silicon Vias) extending through the substrates of the chips.

For example, the external terminals 2 are connected with elements in the control chip 20 via lands 3, bumps 4, TSVs 5, and multi-layer lines 21. The external terminals 2 are provided immediately under the basal plate 1 and electrically connected to the lands 3. The lands 3 extend through the basal plate 1 from its lower surface to its upper surface. The TSVs 5 extend through the substrate 22 of the control chip 20 from the underside to the front side and electrically connect the bumps 4 and the multi-layer lines 21.

The external terminals 2 are connected with elements in the memory chip 10-1 via the lands 3, the bumps 4, the TSVs 5, the multi-layer lines 21, bumps 6, and multi-layer lines 11-1. The bumps

~~CLAIMS~~

What is claimed is:

~~[Claim 1.]~~ A storage device comprising:

a control chip; and

a plurality of memory chips;

wherein the control chip has an input buffer common to the control chip and the plurality of memory chips and electrically connected to an external terminal,

a first transmission path going through the input buffer and a second transmission path not going through the input buffer are provided between the external terminal and the plurality of memory chips, and

in a first mode, the control chip enables the input buffer so as to activate the first transmission path and, in a second mode, disables the input buffer so as to activate the second transmission path.

~~[Claim 2.]~~ The storage device according to claim 1, wherein

the first mode includes an operation mode in which a control signal is supplied from the external terminal to a control circuit in each of the control chip and the plurality of memory chips using the first transmission path, and

the second mode includes a test mode in which the operation of each of the control chip and the plurality of memory chips is checked using the second transmission path.

~~[Claim 3.]~~ The storage device according to claim 1, wherein

the control chip has a first control circuit that, in the first mode, enables the input buffer and that, in the

second mode, disables the input buffer.

~~[Claim 4.]~~ The storage device according to claim 3, wherein

the control chip further has a first transfer switch provided on the second transmission path and electrically connected to the external terminal,

in the first mode, the first control circuit maintains the first transfer switch in an off state and, in the second mode, turns on the first transfer switch, and

each of the plurality of memory chips has:

a second transfer switch provided on the second transmission path and electrically connected to the external terminal; and

a second control circuit that, in the first mode, maintains the second transfer switch in the off state and, in the second mode, turns on the second transfer switch.

~~[Claim 5.]~~ The storage device according to claim 3, wherein

the control chip further has a first transfer switch provided on the second transmission path and electrically connected to the external terminal,

in the first mode, the first control circuit maintains the first transfer switch in an off state and, in the second mode, turns on the first transfer switch, and

each of the plurality of memory chips has:

a second transfer switch provided on the second transmission path;

a connection switch provided on the second transmission path and that electrically connects the external terminal to the second transfer switch; and

a second control circuit that, in the first mode,

maintains at least the connection switch in the off state and, in the second mode, turns on the connection switch and the second transfer switch.

~~[Claim 6.]~~ The storage device according to claim 3, wherein

the control chip further has a first transfer switch provided on the second transmission path,

in the first mode, the first control circuit maintains the first transfer switch in an off state and, in the second mode, turns on the first transfer switch, and

each of the plurality of memory chips has:

a second transfer switch provided on the second transmission path;

a connection switch provided on the second transmission path and that electrically connects the external terminal to each of the first transfer switch and the second transfer switch; and

a second control circuit that, in the first mode, maintains at least the connection switch in the off state and, in the second mode, turns on each of the connection switch and the second transfer switch.

~~[Claim 7.]~~ A storage device comprising:

a control chip; and

a plurality of memory chips stacked on the control chip,

wherein the control chip has an output driver that outputs signals of the plurality of memory chips to an output terminal.

~~[Claim 8.]~~ The storage device according to claim 7, wherein

the control chip further has a drive circuit that transfers signals transferred from the plurality of memory chips to the output driver.

~~[Claim 9.]~~ The storage device according to claim 7, wherein

each of the plurality of memory chips puts together a signal of the memory chip and a signal transferred from the memory chip adjacent above to transfer to the memory chip adjacent below, and

the output driver outputs a signal according to a signal transferred from the memory chip that is the lowest of the plurality of memory chip to the output terminal.

~~[Claim 10.]~~ The storage device according to claim 7, wherein

a signal line is connected, as a common signal line, to the plurality of memory chips, and a signal of each memory chip is outputted onto the common signal line via a second driver,

the control chip further has a drive circuit that includes a first current source electrically connected between a power supply potential and the common signal line, and

the output driver is electrically connected between the common signal line and the output terminal.

~~[Claim 11.]~~ The storage device according to claim 7, wherein

a signal line is connected, as a common signal line, to the plurality of memory chips, and a signal of each memory chip is outputted onto the common signal line via a third driver,

the control chip further has a drive circuit that includes a second current source electrically connected between a reference potential and the common signal line, and

the output driver is electrically connected between the common signal line and the output terminal.