

PATENT SPECIFICATION

(11) 1376 639

1376 639

- (21) Application No. 15571/72 (22) Filed 5 April 1972
 (31) Convention Application No. 131721 (32) Filed 6 April 1971
 (31) Convention Application No. 131722 (32) Filed 6 April 1971 in
 (33) United States of America (US)
 (44) Complete Specification published 11 Dec. 1974
 (51) International Classification H01L 5/00//3/00
 (52) Index at acceptance

HIK 211 21Y 223 22Y 312 413 41Y 422 455 462 469
 470 473 475 477 479 480 491 50X 511 515 51Y
 520 578 579 581 639 650

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(54) IMPROVEMENTS IN OR RELATING TO CHARGE COUPLED DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195 Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to charge coupled devices.

The charge coupled device concept is now well known in the art. Our Great Britain co-pending applications nos. 21832/71 (serial no. 1340619), 21830/71 (serial no. 1340617), 29656/71 (serial no. 1356629), and 58214/71 (serial no. 1358890) describe various aspects of such devices.

One impediment to high charge transfer efficiency in charge coupled devices is the presence of surface states at the semiconductor-insulator interface. Charge representing information is stored and transferred at this interface and the surface states cause trapping of charge so that after a finite number of transfer operations (which may be undesirably low) the information must be regenerated or the line terminated. Intense efforts have been devoted to overcoming this problem.

It has also been known since the earliest proposals of these devices that the charge transfer speed in a device with standard configuration is diffusion limited. Methods for enhancing the transfer rate by using drift fields were described in the first of the above-mentioned applications and although the field profiles proposed then are obtainable and are significant in terms of achieving accelerated transfer, the specific mode of producing the field patterns via thick insulating layers is not always

desirable. In this case, again, the storage and transfer of charge is at the semiconductor-insulator interface.

In fabricating charge coupled devices, it has generally been found necessary to space adjacent storage sites very closely. This avoids blocking of charge transfer due to the potential barrier that often occurs in conventional structures when the interelectrode space is too large. It has been found that efficient, high-density, charge coupled devices often require electrode patterns that are difficult to provide by current commercial processing.

According to this invention there is provided a charge coupled device including a semiconductor charge carrier storage layer bounded on a major plane thereof by a rectifying barrier, and means for applying an electrical bias to said layer, said device being such that, in use with said layer appropriately biased, stored information-representative charge carriers are confined to the interior of said layer and are controllably moveable between discrete storage sites in said layer.

The said storage layer may overlie a semiconductor layer of the opposite conductivity type and form a p-n junction therewith, a plurality of drive electrodes may define said discrete storage sites, and there may be provided means for applying energisation to said electrodes for moving said charge carriers.

In one embodiment of the invention said electrodes are situated on a first insulating layer on said storage layer. There may be provided a second insulating layer overlying said electrodes, a conductive layer overlying said second insulating layer, and means for applying bias to said conductive layer.

In another embodiment of the invention each of said drive electrodes is on and forms a Schottky barrier with said storage layer. The portions of said storage layer between said

electrodes may be covered by insulating material. The said drive electrodes may be of Cu, Mo, W, Ni, the six-platinum group metals (Os, Ru, Ir, Pd, Pt, RL) or mixtures thereof, and each of said Schottky barriers may comprise a metal silicide-silicon interface.

In yet another embodiment of the invention each of said drive electrodes is on a respective discrete impurity region formed in and of the opposite conductivity type to said storage layer. The said storage layer may be n-type conductivity and the doping density thereof may be greater than that of said layer it overlies.

In a further embodiment of the invention said major and the opposite plane of said storage layer are bounded by isolating semiconductor layers of opposite conductivity type to that of said storage layer, a plurality of drive electrodes situated on an insulating layer on one of said isolating layers define said discrete storage sites, and there is provided means for applying energisation to said electrodes for moving said charge carriers. There may be provided a further semiconductor charge carrier storage layer bounded on a major plane thereof by one of said isolating layers and on the opposite plane by another semiconductor isolating layer of said opposite conductivity type, and means for applying an electrical bias to said further storage layer with respect to the isolating layers bounding its said planes. There may be provided means for interconnecting said storage layers.

In devices in accordance with the invention the carriers encounter only bulk trapping sites, and since these are characteristically far less prevalent than surface states, the charge transfer efficiency can be increased. Also, it is possible to create field gradations for accelerating charge transfer, so that the speed of the device is limited by the drift velocity of carriers rather than the diffusion velocity. With the storage volume within the storage medium, the field profile can be tailored with relative flexibility by adjusting the electrode area and the interelectrode spacing. Another advantage is that the electrodes can be spaced at distances well within the state of the micro-circuit art.

The invention will now be described by way of example with reference to the accompanying drawings, in which:

Fig. 1A is an energy level diagram of a charge coupled device in an unbiased condition;

Fig. 1B is an energy level diagram of the same device after biasing to remove the free carriers;

Fig. 2 is an energy level diagram of an alternative device in which the storage layer is terminated on each side with a metal-insulator barrier;

Fig. 3 is an energy level diagram of another

alternative device with a buried channel for the storage of charge;

Fig. 4 is an energy level diagram of another device having two buried channels;

Fig. 5 is a schematic sectional view of one form of single channel device having the electrical configuration represented by Figs. 1A and 1B;

Fig. 6 is a schematic sectional view indicating field enhancement;

Fig. 7 is a schematic sectional view of a device similar to that of Fig. 5 but with provision for compensating for charge trapping at the large potential wells that form between the field plates;

Fig. 8 is a schematic sectional view of another device in which the storage layer is isolated from the drive electrodes with Schottky barriers, and

Fig. 9 is a schematic sectional view of yet another device in which the storage layer is isolated from the drive electrodes with p-n junctions.

Referring to the energy level diagram of Fig. 1A, a layer 10 is a conventional metal electrode used to control storage and transfer of the charge carriers. Layer 11 is a standard insulating layer. A semiconductor layer normally completes the MIS structure. In the usual charge coupled device storage and transfer of charge occurs at the semiconductor-insulator interface. As pointed out above, this heterogeneous region is not a favourable location for this. In the present device, the energy minimum that normally attracts charge to the interface is shifted to a homogeneous layer that intervenes between the semiconductor and the insulator. In Fig. 1 the usual n-layer is represented at 12. The intervening storage layer appears at 14 and the barrier, in this case a p-n junction, occurs at 13. It should be evident that whenever conductivity types are indicated, the complementary configuration can be used as well.

Fig. 1A shows the device in thermal equilibrium with the free positive charge in the p-layer associated with fixed negative charge as shown.

In Fig. 1B the free charge has been removed from the p-layer by simply biasing this layer with a voltage negative with respect to the n-layer 12. With proper design as set forth below, the result is that residual negative charge bends the energy bands as shown and leaves a buried channel for positive charge in the middle of the storage layer. Thus, when free positive charge, such as hole 15, is intentionally introduced into the storage medium, it will physically drift to the allowed state of minimum potential, at a distance W corresponding to the channel depth, and thus will be electrically confined to the interior of layer 14.

In the diagram shown in Fig. 2 a semiconductor storage medium 20 is bounded on

both planar faces with a metal-insulator barrier, 21—22 and 23—24, respectively. When the storage layer 20 is depleted of carriers the band structure in the storage medium 20 is qualitatively equivalent to that of layer 14 in Fig. 1A.

In Fig. 3 the storage medium is isolated on both sides with a p-n junction. Again the basic structure is metal-insulator-semiconductor with a conventional metal layer 30 and an insulator layer 31. The semiconductor, however, is an n-p-n structure comprising n-layer 32, p-layer 33 (the storage layer) and n-layer 34. The band structure of layer 33, after depletion of free carriers, resembles that in the other devices.

It should be apparent that the n-p-n structure of Fig. 3 can be extended to provide dual channel operation on both sides of a single device by providing parallel buried channels through dual layer isolation. For example, using a n-p-n-p-n structure, two parallel p-channels are isolated. Interconnection between channels can be provided.

The diagram of Fig. 4 shows two isolated parallel channels using simply a p-n-p structure. The two p-type storage layers 40 and 41 are isolated in the interior region by an n-layer 42. The other boundaries are MIS barriers formed by metal layers 43, 44 and insulating layers 45, 46. The curved band structure of the storage layers is evident. It will also be appreciated that, inherent in the dual plane channel structure just described is the potential for constructing electrical cross-overs and interconnections and for obtaining structures resembling, functionally, those described in Great Britain copending application no. 58214/71 (serial no. 1358890).

Referring now to Fig. 5, a storage layer 50, which is shown as p-type semiconductor, and preferably is silicon with a normal resistivity (0.1 to 100 ohm cm), is bounded on the surface with the usual insulating layer 51 and is further isolated at its lower boundary by a p-n junction 52 formed in the conventional way and including an n-layer 53. The device shown as control electrodes 54, 55 and 56 connected to a conventional three wire drive comprising wires 57, 58 and 59 (illustrated schematically). Bias means 60 is shown schematically and is intended to bias, via an electrode 61, the storage layer 50 with respect to n-layer 53 so that the carriers in the storage layer are essentially removed. Electrode 61 may comprise a Schottky contact, or a p⁺ region 62 may be provided to allow ohmic contact. The device is then in condition for normal charge coupled operation except that the information carriers will now be stored and transferred in the bulk of the storage layer as indicated schematically in the figure.

Field enhancement of the charge transfer process is illustrated in Fig. 6. The storage medium 50 is structurally the same as that in

Fig. 5. With a voltage V impressed on electrode 54 and a larger voltage, e.g., 2V, impressed on electrode 55, the field profile will approximate that suggested schematically by the dashed line 63. Since the carriers are now located within the bulk of the storage layer, they can be influenced by the field gradient. In the normal charge transfer process the carriers are located so near to the interface between layers 50 and 51 that an effective field gradient may require an inordinately thick insulating layer or inordinately small electrodes and spacing.

In the devices of Figs. 5 and 6 the electrode spacing is larger than is encountered with an ordinary charge coupled device and this is possible by virtue of the present invention.

However, just as in the former devices, large interelectrode spacing leads to "blocking" of charge, this time due to large potential wells that form between the electrodes. Although it is not immediately evident from the foregoing description, experiments have shown that charge injected into a storage layer of the kind described in connection with Fig. 5 does not distribute uniformly due to the presence of the metal field plates. The regions between the field plates have lower potential energies and attract charge. Therefore it is helpful to incorporate fixed charge into the structure to overcome this. In the configuration described in connection with Figs. 5 and 6 the regions between the field plates attract positive charge. This can be compensated by introducing fixed positive charge in or near those regions. A convenient way for accomplishing this is to implant positive ions into the insulating layer and/or the semiconductor between the electrodes using the latter as a mask. The mechanics of doing this are well known. The amount of charge should be sufficient to establish approximately a uniform electric field along the semiconductor surface when a bias equivalent to the storage bias is applied to the field plates. This can be calculated in a simple model using the relation.

$$P = \epsilon E$$

where P is the necessary polarization in coulombs/cm², ϵ is the dielectric constant of the insulator, and E is the electric field. In this case E should approximate the electric field under the field plate, or V/d where V is the storage voltage on the field plate and d is the thickness of the insulator under the field plate.

Another way of compensating for these large interelectrode potential wells is shown in Fig. 7. This section is a portion of the device of Fig. 5 and is similar in detail except for the provision of a continuous field plate 70 extending along the entire active surface. The field plate 70 is insulated from the drive elec-

trodes by an insulating layer 71. Since the metal plate 70 is nearer to the semiconductor in the regions between the electrodes a positive voltage placed on the electrode 70 via voltage source 72 will be equivalent to placing fixed positive charge at the semiconductor-insulator interface as just described. Appropriate voltages and insulating layer thicknesses can be obtained from the expressions discussed above.

A preferred method for overcoming the deep inter-electrode wells is to use a four-layer metallization as described in detail in Great Britain copending application no. 49603/71 (serial no. 1344646).

It should be pointed out that the p-n-p structures or, in general, forms in which the storage layer is isolated with a p-n junction on both sides, do not suffer from this problem.

Referring again to Fig. 6, experiments have shown that for effective field aided transfer, the average electrode dimension X_p , is preferably related to the dimension W by the following:

$$\frac{1}{100} < \frac{W}{X_p} < 10.$$

It is evident that the dimension W includes the thickness of the insulating layer. This layer should be thick enough to avoid dielectric breakdown but yet sufficiently thin to allow for practical drive voltages on the control elements. For silicon dioxide on silicon a desirable range is 0.02 to 1 micron. More specifically, if the SiO_2 layer is 0.1 micron thick and the carrier concentration in a storage layer 5μ thick is of the order of $10^{15}/\text{cm}^3$ then appropriate drive voltages fall in the useful range of 0—50 volts, e.g., 0, 5 and 10 volts on the three-wire drive system.

Appropriate impurity concentrations can be prescribed in terms of the thickness of the storage layer as follows:

To avoid breakdown, the doping density, N_A , in cm^{-3} , in the storage layer is given by the approximate expression.

$$N_A \leq \left(\frac{6.6 \times 10^{19} (E_g/1.1)^{3/2} K_s}{W^2} \right)^{4/7}$$

where E_g is the band gap in eV, K_s the dielectric constant and W the depth of the channel. For silicon

$$N_A \leq \left(\frac{8 \times 10^{20}}{W^2} \right)^{4/7}$$

If a channel depth of 10^{-3} cm is assumed by way of example then the maximum carrier concentration N_A is $2.5 \times 10^{15}/\text{cm}^3$. The lower limit is ordinarily established by the intrinsic carrier concentration.

From the standpoint of maintaining the charge that represents the information isolated from the surface states it would normally be sufficient if the storage medium is such that the energy difference between the stored carriers in the bulk and the surface states is too large to be overcome by thermal excitation. The specific energy difference is simply the Boltzmann expression kT . In a structural sense this means that carriers stored in silicon will ordinarily reside physically at a depth of at least 30Å from the silicon-insulator interface. This distance is generally of the order of 0.01 to 10 microns.

With reference to the symbols appearing in Fig. 6, the following specific values are given by way of example:

$$\begin{aligned} X_s &= 1 \times 10^{-3} \text{ cm} \\ X_p &= 1 \times 10^{-3} \text{ cm} \\ Y_i &= 1 \times 10^{-5} \text{ cm} \\ Y_s &= 5.0 \times 10^{-4} \text{ cm} \\ N_A &= 2 \times 10^{15} \text{ cm}^{-3} \\ N_D &= 10^{14} \text{ cm}^{-3} \\ V &= 5 \text{ volts} \\ V_B &= 20 \text{ volts} \\ W &= 4 \times 10^{-4} \text{ cm.} \end{aligned}$$

The devices shown in Figs. 8 and 9 take advantage of the recognition that when a Schottky barrier or p-n junction is used for isolating the channel from the electrode, the usual intervening insulating layer, e.g., layer 31 in Fig. 3, is not essential from a functional standpoint. Thus, in Fig. 8, metal electrodes 81—83 can be placed directly on the semiconductor storage layer 84. The storage layer is isolated on the buried side by substrate 85 forming p-n junction 86. The electrodes form nonohmic contacts so that the electrode 87, used to bias the storage layer via source 88, requires a more highly doped region 89 similar to region 62 in Fig. 6. The exemplary three-phase drive is shown as before. The metal electrodes 81 to 83 may comprise any of several metals forming Schottky barriers with the substrate. In the case of silicon, appropriate metals are Cu, Mo, Ni, W, any of the six platinum group metals (Os, Ru, Ir, Pd, Pt, Rh) or mixtures thereof. Formation of these barriers is described in the Bell System Technical Journal, Vol. XLIV, No. 7, Sept. 1965. The thickness of the electrodes is not critical. As a consequence of normal fabrication techniques, the metal electrodes are formed within windows of an insulating layer 90.

In Fig. 9 isolation is achieved via p-n junctions. The configuration is essentially identical to that of Fig. 8 with prime numbers corresponding to the respective elements in Fig. 8 except for the diffused p-regions 91 underlying each drive electrode. The p-regions can be formed by diffusion through the windows of the oxide prior to formation of the metal, by

diffusion from doped metal contacts, or by implantation either prior to formation of the electrodes or implantation through the electrodes if the relative ion transparency of the electrodes with respect to the insulating layer is favourable. The device of Fig. 9, having p-n junction isolation rather than MOS or Schottky barriers, has the advantage that thermal generation currents are low.

In Figs. 8 and 9 the n- and p-layers are complementary to those of Figs. 1-7. Possible doping parameters for this configuration are the following:

$$N_A = 10^{14}/\text{cm}^3,$$

$$N_D = 10^{18}/\text{cm}^3,$$

$$\text{depth of n-layer} = 10^{-4} \text{ cm.}$$

It is preferred that the doping density of the substrate be less than that of the n-layer.

WHAT WE CLAIM IS:—

1. A charge coupled device including a semiconductor charge carrier storage layer bounded on a major plane thereof by a rectifying barrier, and means for applying an electrical bias to said layer, said device being such that, in use with said layer appropriately biased, stored information-representative charge carriers are confined to the interior of said layer and are controllably moveable between discrete storage sites in said layer.

2. A device as claimed in claim 1 wherein said storage layer overlies a semiconductor layer of the opposite conductivity type and forms a p-n junction therewith, a plurality of drive electrodes define said discrete storage sites, and there is provided means for applying energisation to said electrodes for moving said charge carriers.

3. A device as claimed in claim 2 wherein said electrodes are situated on a first insulating layer on said storage layer.

4. A device as claimed in claim 3 including a second insulating layer overlying said electrodes, a conductive layer overlying said second insulating layer, and means for applying bias to said conductive layer.

5. A device as claimed in claim 1 wherein said major and the opposite plane of said storage layer are bounded by isolating semiconductor layers of opposite conductivity type to that of said storage layer, a plurality of

drive electrodes situated on an insulating layer on one of said isolating layers define said discrete storage sites, and there is provided means for applying energisation to said electrodes for moving said charge carriers.

6. A device as claimed in claim 5 including a further semiconductor charge carrier storage layer bounded on a major plane thereof by one of said isolating layers and on the opposite plane by another semiconductor isolating layer of said opposite conductivity type, and means for applying an electrical bias to said further storage layer with respect to the isolating layers bounding its said planes.

7. A device as claimed in claim 6 including means for interconnecting said storage layers.

8. A device as claimed in claim 2 wherein each of said drive electrodes is on and forms a Schottky barrier with said storage layer.

9. A device as claimed in claim 8 wherein the portions of said storage layer between said electrodes are covered by insulating material.

10. A device as claimed in claim 8 or 9 wherein said drive electrodes are of Cu, Mo, W, Ni, the six platinum group metals (Os, Ru, Ir, Pd, Pt, Rh) or mixtures thereof, and each of said Schottky barriers comprises a metal silicide-silicon interface.

11. A device as claimed in claim 2 wherein each of said drive electrodes is on a respective discrete impurity region formed in and of the opposite conductivity type to said storage layer.

12. A device as claimed in claim 8, 9, 10 or 11 in which said storage layer is n-type conductivity.

13. A device as claimed in claim 12 in which the doping density of said storage layer is greater than that of said layer it overlies.

14. A charge coupled device arranged and adapted to operate substantially as herein described with reference to Fig. 1, 2, 3, 4, 5, 6 or 7 of the accompanying drawings.

15. A charge coupled device arranged and adapted to operate substantially as herein described with reference to Fig. 8 or 9 of the accompanying drawings.

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In Figs. 8 and 9 the n- and p-layers are complementary to those of Figs. 1-7. Possible doping parameters for this configuration are the following:

$$N_A = 10^{14}/\text{cm}^3,$$

$$N_D = 10^{16}/\text{cm}^3,$$

$$\text{depth of n-layer} = 10^{-4} \text{ cm.}$$

It is preferred that the doping density of the substrate be less than that of the n-layer.

WHAT WE CLAIM IS:—

1. A charge coupled device including a semiconductor charge carrier storage layer bounded on a major plane thereof by a rectifying barrier, and means for applying an electrical bias to said layer, said device being such that, in use with said layer appropriately biased, stored information-representative charge carriers are confined to the interior of said layer and are controllably moveable between discrete storage sites in said layer.

2. A device as claimed in claim 1 wherein said storage layer overlies a semiconductor layer of the opposite conductivity type and forms a p-n junction therewith, a plurality of drive electrodes define said discrete storage sites, and there is provided means for applying energisation to said electrodes for moving said charge carriers.

3. A device as claimed in claim 2 wherein said electrodes are situated on a first insulating layer on said storage layer.

4. A device as claimed in claim 3 including a second insulating layer overlying said electrodes, a conductive layer overlying said second insulating layer, and means for applying bias to said conductive layer.

5. A device as claimed in claim 1 wherein said major and the opposite plane of said storage layer are bounded by isolating semiconductor layers of opposite conductivity type to that of said storage layer, a plurality of

drive electrodes situated on an insulating layer on one of said isolating layers define said discrete storage sites, and there is provided means for applying energisation to said electrodes for moving said charge carriers.

6. A device as claimed in claim 5 including a further semiconductor charge carrier storage layer bounded on a major plane thereof by one of said isolating layers and on the opposite plane by another semiconductor isolating layer of said opposite conductivity type, and means for applying an electrical bias to said further storage layer with respect to the isolating layers bounding its said planes.

7. A device as claimed in claim 6 including means for interconnecting said storage layers.

8. A device as claimed in claim 2 wherein each of said drive electrodes is on and forms a Schottky barrier with said storage layer.

9. A device as claimed in claim 8 wherein the portions of said storage layer between said electrodes are covered by insulating material.

10. A device as claimed in claim 8 or 9 wherein said drive electrodes are of Cu, Mo, W, Ni, the six platinum group metals (Os, Ru, Ir, Pd, Pt, RL) or mixtures thereof, and each of said Schottky barriers comprises a metal silicide-silicon interface.

11. A device as claimed in claim 2 wherein each of said drive electrodes is on a respective discrete impurity region formed in and of the opposite conductivity type to said storage layer.

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13. A device as claimed in claim 12 in which the doping density of said storage layer is greater than that of said layer it overlies.

14. A charge coupled device arranged and adapted to operate substantially as herein described with reference to Fig. 1, 2, 3, 4, 5, 6 or 7 of the accompanying drawings.

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