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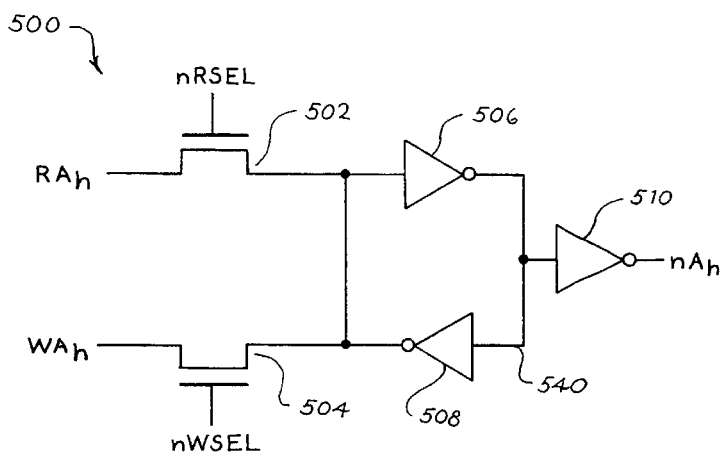
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- (71) Applicants: **ADVANCED MICRO DEVICES, INC.** [US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US). **FUJITSU LIMITED** [JP/JP]; 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa 211 (JP). Published:
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- (72) Inventors: **AKAOGI, Takao**; 7911 October Way, Cupertino, CA 95014 (US). **NGUYEN, Kendra**; 4942 Zeppelin

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(54) Title: MULTIPLE BANK SIMULTANEOUS OPERATION FOR A FLASH MEMORY



(57) Abstract: An address buffering and decoding architecture for a multiple bank (or N bank) simultaneous operation flash memory is described. For the duration of a read operation at one bank of the N banks, a write operation can only be performed on any one of the other N-1 banks. For the duration of a write operation at one bank of the N banks, a read operation can only be performed on any one of the other N-1 banks. The address buffering and decoding architecture includes a control logic circuit (218), an address selection circuit located at each of the N banks, and address buffer circuitry (220). The control logic circuit (218) is used to generate N read select signals to select one bank of the N banks for a read operation and N write select signals to selection another bank of the N banks for a write operation. Each address select circuit is configured to receive from the control logic circuit (218) a respective one of the N read select signals and a respective one of the N write select signals. The address buffer circuitry (220) is used to simultaneously provide a write address and a read address in order to access core memory cells. Respective first portions of the write and read addresses are provided to the control logic circuit (218) to generate the respective N read select signals and N write select signals. Respective second portions of the write and read addresses are provided to the respective address selection circuit.