ABSTRACT

A NOVEL METHOD OF FORMING CONTACT TO POLYSILICON GATE FOR MOS DEVICES

A new method is provided for the creation of contact pads to the poly gate of MOS devices. STI regions are formed, layers of gate oxide, poly and SiN are deposited. The poly gate is patterned and etched leaving a layer of SiN on the surface of the gate. An oxide liner is created, an LDD implant is performed, the gate spacers are created and source/drain region implants are performed. A layer of titanium is deposited and annealed, a salicide etchback is performed to the layer of titanium creating silicided surfaces over the source and drain regions. Inter level dielectric (ILD) is deposited, the layer of ILD is polished down to the SiN layer on the top surface of the gate. The layer of SiN is removed creating a recessed gate structure.

A stack of layers of titanium-amorphous silicon-titanium (Ti/Si/Ti) or a layer of WSi_x is deposited over the layer of ILD filling the recess on top of the gate with Ti/Si/Ti. This Ti/Si/Ti (or WSi_x) is patterned and etched forming a Ti/Si/Ti stack (or layer of WSi_x) that partially overlays the layer of ILD while also penetrating the recessed opening of the gate electrode. The layer of Ti/Si/Ti is silicided and forms the contact pad to the gate structure.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)