CLAIMS:

1. A heterogeneous-chip package, comprising:

a base die surrounded by a molding material, the base die comprising first interconnections, and through interconnections;

a metal post in and contacting the molding material, the metal post laterally spaced apart from the base die;

a first chip electrically coupled to the base die;

a second chip electrically coupled to the base die, the second chip electrically coupled to the first chip by at least one of the first interconnections in the base die;

a dielectric material between and in contact with the first chip and the second chip;

a silicon die vertically beneath the base die; and

second interconnections below the base die, the second interconnections laterally spaced apart from the silicon die.

2. The heterogeneous-chip package of claim 1, wherein the base die is in contact with the molding material.

3. The heterogeneous-chip package of claim 1, wherein the first chip and the second chip are entirely within a footprint of the base die.

4. The heterogeneous-chip package of claim 1, wherein the silicon die is only partially within a footprint of the base die.

5. The heterogeneous-chip package of claim 1, wherein the silicon die is electrically coupled to the base die.

6. The heterogeneous-chip package of claim 1, wherein the silicon die has external terminations on only a top side of the silicon die.

7. The heterogeneous-chip package of claim 1, wherein the metal post is a fiducial.

8. A heterogeneous-chip package, comprising:

a first die having a first sidewall and a second sidewall, the second sidewall laterally opposite the first sidewall, the first die comprising first interconnections, and through interconnections;

a molding material laterally adjacent to the first sidewall and the second sidewall of the first die;

a metal post in and contacting the molding material, the metal post laterally spaced apart from the first die;

a second die conductively coupled to the first die;

a third die conductively coupled to the first die, the third die conductively coupled to the second die by at least one of the first interconnections of the first die;

a dielectric material between and in contact with the second die and the third die; and

second interconnections below the first die.

9. The heterogeneous-chip package of claim 8, further comprising:

a fourth die vertically beneath the first die, wherein the second interconnections are laterally spaced apart from the fourth die, and wherein the fourth die has contacts on only a top side of the fourth die.

10. The heterogeneous-chip package of claim 9, wherein the fourth die is only partially within a footprint of the first die.

11. The heterogeneous-chip package of claim 8, wherein the molding material is in contact with the first sidewall and the second sidewall of the first die.

12. The heterogeneous-chip package of claim 8, wherein the second die and the third die are entirely within a footprint of the first die.

13. The heterogeneous-chip package of claim 8, wherein the metal post is a fiducial for accurately placing the first die.

14. A heterogeneous-chip package, comprising:

a base die having a first sidewall and a second sidewall between a top side and a bottom side, the second sidewall laterally opposite the first sidewall, the base die comprising interconnections on the top side of the base die and interconnections on the bottom side of the base die, wherein one or more of the interconnections on the top side of the base die are coupled to corresponding ones of the interconnections on the bottom side of the base die;

a molding material laterally adjacent to the first sidewall and the second sidewall of the base die;

a metal post laterally spaced apart from the base die, the metal post having a sidewall in contact with the molding material;

a first chip vertically over and coupled to the base die;

a second chip vertically over and coupled to the base die, the second chip laterally spaced apart from the first chip, and the second chip coupled to the first chip by an interconnection of the top side of the base die;

a dielectric material between a sidewall of the first chip and a sidewall of the second chip, the dielectric material in contact with the sidewall of the first chip and the sidewall of the second chip;

a silicon die vertically beneath the base die, the silicon die having external terminations on only a top side of the silicon die; and

second interconnections below the base die, the second interconnections laterally spaced apart from the silicon die.

15. The heterogeneous-chip package of claim 14, wherein the molding material is in contact with the first sidewall and the second sidewall of the base die.

16. The heterogeneous-chip package of claim 14, wherein the first chip and the second chip are entirely within a footprint of the base die.

17. The heterogeneous-chip package of claim 14, wherein the silicon die is only partially within a footprint of the base die, and wherein the silicon die is electrically coupled to the base die.

18. The heterogeneous-chip package of claim 14, wherein the metal post is a fiducial.

19. The heterogeneous-chip package of claim 14, wherein the silicon die bridges the base die to a second base die.

20. The heterogeneous-chip package of claim 14, wherein the dielectric material has an uppermost surface at a same level as an uppermost surface of the first chip and as an uppermost surface of the second chip.