

WHAT IS CLAIMED IS:

1. A semiconductor package, comprising:
a semiconductor chip on a package substrate; and
an under-fill layer between the semiconductor chip and the package substrate,
wherein the semiconductor chip includes:
a semiconductor substrate;
an interlayer dielectric layer on the semiconductor substrate and including a plurality of connection lines;
a plurality of conductive pads on the interlayer dielectric layer, first ones of the plurality of conductive pads being electrically connected to first ones of the plurality of connection lines, respectively, and second ones of the plurality of conductive pads being electrically isolated from the plurality of connection lines;
a passivation layer on the interlayer dielectric layer and including a plurality of first holes, the plurality of first holes on the first ones of the plurality of conductive pads and the second ones of the plurality of conductive pads, respectively; and
a plurality of first conductive bumps bonded to the first ones of the plurality of conductive pads, respectively,
wherein the under-fill layer includes a first portion, and the first portion is in a first one of the plurality of first holes and is in contact with a first conductive pad of the second ones of the plurality of conductive pads,
wherein the passivation layer further includes a second hole spaced apart from the plurality of first holes, and
wherein a depth of the second hole is greater than each of respective depths of the plurality of first holes.
2. The semiconductor package of claim 1, further comprising a second

conductive bump bonded to a second conductive pad of the second ones of the plurality of conductive pads.

3. The semiconductor package of claim 1 or claim 2, wherein the plurality of conductive pads further includes a third conductive pad that is electrically connected to a second one of the plurality of connection lines, and

wherein the under-fill layer includes a second portion, and the second portion is in a second one of the plurality of first holes and is in contact with the third conductive pad.

4. The semiconductor package of claim 3, wherein the semiconductor chip further includes a test circuit, and the test circuit is connected to the third conductive pad and is in the interlayer dielectric layer.

5. The semiconductor package of claim 1 or claim 2, wherein the plurality of conductive pads further includes a third conductive pad that is electrically connected to a second one of the plurality of connection lines, and

wherein the semiconductor package further includes a third conductive bump that extends through the passivation layer and is bonded to the third conductive pad.

6. The semiconductor package of any one of claims 1 to 5, wherein the second hole extends partially into the passivation layer in a thickness direction of the passivation layer.

7. A semiconductor package, comprising:
a semiconductor chip on a package substrate,
wherein the semiconductor chip includes:

a semiconductor substrate;

an interlayer dielectric layer on the semiconductor substrate and including a plurality of connection lines;

a plurality of conductive pads on the interlayer dielectric layer, first ones of the plurality of conductive pads being electrically connected to first ones of the plurality of connection lines, and second ones of the plurality of conductive pads being electrically isolated from the plurality of connection lines; and

a passivation layer on the interlayer dielectric layer,

wherein the passivation layer includes a plurality of first holes and a second hole,

wherein ones of the plurality of first holes are on the first ones of the plurality of conductive pads and the second ones of the plurality of conductive pads, respectively, and

wherein the second hole does not vertically overlap any of the first ones of the plurality of conductive pads and does not vertically overlap any of the second ones of the plurality of conductive pads, and

wherein each of the plurality of first holes has a first depth, the second hole has a second depth, and

the second depth is greater than the first depth.

8. The semiconductor package of claim 7, wherein the second hole does not extend through the passivation layer.

9. The semiconductor package of claim 7 or claim 8, wherein the semiconductor chip further includes a second conductive bump bonded to one of the second ones of the plurality of conductive pads.

10. The semiconductor package of any one of claims 7 to 9, wherein the plurality of conductive pads further includes a third conductive pad that is electrically connected to a second one of the plurality of connection lines, and

wherein the semiconductor package further includes a third conductive bump that extends through the passivation layer and is bonded to the third conductive pad.

11. The semiconductor package of any one of claims 7 to 9, further comprising an under-fill layer between the package substrate and the semiconductor chip,

wherein the plurality of conductive pads further includes a third conductive pad that is electrically connected to a second one of the plurality of connection lines,

wherein one of the plurality of first holes of the passivation layer is on the third conductive pad, and

wherein the under-fill layer includes a portion that is in the one of the plurality of first holes and that is in contact with the third conductive pad.

12. The semiconductor package of claim 11, wherein the semiconductor chip further includes a test circuit, and the test circuit is connected to the third conductive pad and is disposed in the interlayer dielectric layer.

13. A semiconductor package, comprising:
a first semiconductor chip, a second semiconductor chip, and a third semiconductor chip that are sequentially stacked;

a plurality of first electric conductive bumps and a plurality of first dummy conductive bumps between the first semiconductor chip and the second semiconductor chip;
and

a plurality of second electric conductive bumps and a plurality of second dummy conductive bumps between the second semiconductor chip and the third semiconductor chip,

wherein the plurality of first electric conductive bumps and the plurality of second electric conductive bumps are configured to transmit electrical signals between the first,

second, and third semiconductor chips,

wherein the plurality of first dummy conductive bumps and the plurality of second dummy conductive bumps are electrically floated,

wherein the plurality of first electric conductive bumps and the plurality of second electric conductive bumps include an equal number of electric conductive bumps, and

wherein the plurality of first dummy conductive bumps and the plurality of second dummy conductive bumps include different numbers of dummy conductive bumps,

wherein the second semiconductor chip includes:

a semiconductor substrate;

an interlayer dielectric layer on the semiconductor substrate and including a plurality of connection lines;

a plurality of conductive pads on the interlayer dielectric layer, first ones of the plurality of conductive pads being electrically connected to ones of the plurality of connection lines, respectively, and second ones of the plurality of conductive pads being electrically isolated from the plurality of connection lines; and

a passivation layer on the interlayer dielectric layer and including a plurality of first holes that are on the first ones of the plurality of conductive pads and the second ones of the plurality of conductive pads, respectively,

wherein the passivation layer further includes a second hole spaced apart from the plurality of first holes, and

wherein a depth of the second hole is greater than each of respective depths of the plurality of first holes.

14. The semiconductor package of claim 13, wherein a width of the first semiconductor chip is greater than a width of each of the second and third semiconductor chips.

15. The semiconductor package of claim 13 or claim 14, wherein the first semiconductor chip is a logic chip, and the second semiconductor chip and the third semiconductor chip are memory chips.

16. The semiconductor package of any one of claims 13 to 15, further comprising an under-fill layer between the first semiconductor chip and the second semiconductor chip,

wherein the second semiconductor chip further includes:

a plurality of first conductive bumps bonded to the first ones of the plurality of conductive pads, respectively, and

wherein the under-fill layer includes a portion, and the portion is in one of the plurality of first holes and is in contact with a first conductive pad of the second ones of the plurality of conductive pads.

17. The semiconductor package of claim 16, wherein ones of the first dummy conductive bumps are bonded to second conductive pads of the second ones of the plurality of conductive pads, respectively.

18. The semiconductor package of claim 16 or claim 17, wherein at least one of the plurality of first dummy conductive bumps is bonded to the passivation layer.