



(43) International Publication Date
16 March 2006 (16.03.2006)

(10) International Publication Number
WO 2006/029286 A1

(51) International Patent Classification:

H02M 3/06 (2006.01) *H03K 19/017* (2006.01)
H03K 17/06 (2006.01)

OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL,
SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC,
VN, YU, ZA, ZM, ZW.

(21) International Application Number:

PCT/US2005/032064

(22) International Filing Date: 30 August 2005 (30.08.2005)

(25) **Filing Language:** English

(26) **Publication Language:** English

(30) Priority Data:

60/606,942	3 September 2004 (03.09.2004)	US
10/986,630	12 November 2004 (12.11.2004)	US

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(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ,

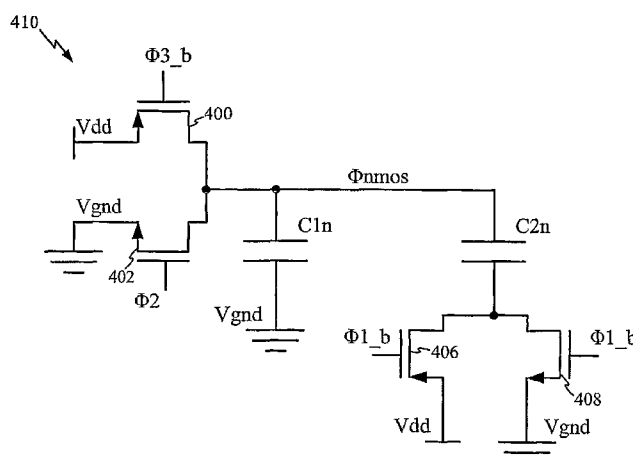
(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LL, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GO, GW, ML, MR, NE, SN, TD, TG)

[Continued on next page]

(54) Title: LOW-VOLTAGE CMOS SWITCH WITH NOVEL CLOCK BOOSTING SCHEME



(S7) Abstract: A method and apparatus for boosting the gate voltages of a CMOS switch used in an integrated circuit designed in a sub-micron CMOS process is disclosed. The CMOS switch is coupled to V_{in} and V_{out} nodes, and contains PMOS and NMOS gates. Two boosting circuits are used to change the voltage on the PMOS and NMOS gates, respectively. The voltage at the NMOS gate is boosted from V_{DD} to $(V_{DD} + K \times V_{DD})$. The voltage at the PMOS gate is decreased from V_{GND} to $(V_{GND} - k \times V_{GND})$. The factor k is chosen such that V_{out} can be sampled through the entire range of $V_{in} = V_{GND}$ to V_{DD} , even where V_{DD} approaches the sum of the absolute values of the threshold voltages of the respective PMOS and NMOS transistors.

WO 2006/029286 A1



- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations

Published:

- with international search report

- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

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