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54. Control circuit for at least one clock electrode of an integrated circuit.

57) The control circuit has two semiconductor switches (PT, NT) which are controllable from a clock pulse generator (CG) via which switches one of two direct voltages ($+V_a$, $0V$) is periodically applied to a clock electrode (E), constituting a capacitive load, of an integrated circuit (IC). To realise a reduced energy dissipation, the clock electrode (ET) is connected to ground via a series arrangement (LC)

of an inductance (L) and a capacitance (C) and a clock pulse supply is effected at which the switches (PT, NT) are successively conducting with an interval thereinbetween in which both switches are non-conducting. As a result, a resonant circuit (L, C, CE) of the inductance (L), the capacitance (C) and the clock electrode capacitance (CE) is active during the intervals.

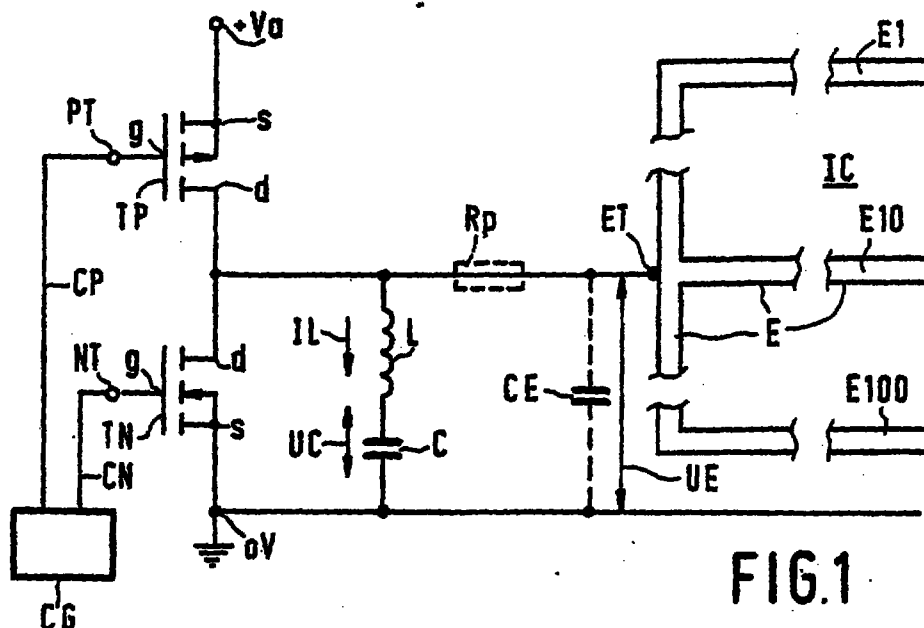


FIG. 1

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