

CONTROLLING GENERATION OF AN ACKNOWLEDGE SIGNAL AND
A BUSY SIGNAL IN AN INTERFACE.

This invention relates generally to a communication
5 control circuit in a system using a parallel interface. In
particular, this invention relates to a circuit for
generating an acknowledge signal and a busy signal,
wherein the above two signals control sending and
receiving of communication data between at least two
10 communication stations, through a Centronics (RTM)
compatible parallel interface.

Generally, a laser printer, for example, using a
Centronics (RTM) compatible parallel interface has a
15 specific data communication method of communicating data
between communication systems, which follows basically the
regulation of the Centronics (RTM) system. For instance,
in a conventional method, when data is transmitted from
another data communication device, strobe signal S_1 output
20 from an Centronics (RTM) interface cable 30 will be
transmitted together with the data communication signal,
as illustrated in Figure 1. If the strobe signal S_1 is
generated, a busy signal S_2 of logic HIGH state will be
generated to prevent transmission of different data until
25 the processing of the data being transmitted currently is
completely executed by a Central Processing Unit (CPU 10).
In this case, the busy signal S_2 is applied to an interrupt
terminal of the CPU 10 so as to inform the CPU 10 of the
receiving of the data. Then, the CPU 10 starts to read in
30 the data received from the other data communication
device and generate an acknowledge signal S_3 from an output
port Y_1 thereof to an acknowledge terminal $\overline{\text{ACK}}$ of the
Centronics (RTM) interface cable 30 in order to send it to
the other data communication device so that the completion

of the data receiving may be indicated to the other data communication device.

At about the same moment, the busy signal S_2 of logic HIGH, generated by the busy signal generator 20, will make a transition from logic HIGH to LOW in order to be ready to receive further data. If the CPU 10 is in a condition in which it is impossible to receive the data, the busy signal S_2 must be returned to logic HIGH again.

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Namely, if the busy signal generator 20 produces the busy signal S_2 under the control of a first control signal S_3 , which controls the generation and release of the busy condition according to the data receiving from the CPU 10, then the busy signal S_2 and a second control signal S_4 , generated from the CPU 10 are provided to an OR gate G_1 , which applies the logical combination result thereof to a busy terminal BUSY of the Centronics (RTM) interface cable 30. In the mean time, the second control signal S_4 is used for generating or releasing the busy condition according to the condition of the CPU 10.

With respect to the timing relation of the acknowledge signal S_3 and busy signal S_2 after the receiving of data when considered in the place of the other data communication device (a transmitter), the busy signal S_2 of the receiver (in this case, the system of Figure 1) becomes the logic LOW state after the transmitter sends out one frame of data. Moreover, if the transmitter receives the acknowledge signal S_3 generated from the receiver, the transmitter will be ready to send another frame of data. It should be noted that these operations are controlled by the CPU 10 by means of software.

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As illustrated in Figure 3, the system shown in Figure 1 receives data at time point t_1 , reads in the data to the CPU 10 at time point t_2 and generates the busy signal S_2 and acknowledge signal S_3 in sequence at time point t_3 , through the output port, so that the system informs the receiver that the system is ready to receive the next data.

Therefore, the transmitter transmits the next data at the instance of time point t_3 and again the CPU 10 of the receiver is provided with the busy signal S_2 generated by the busy signal generator 20. In the mean time, according to the conventional method as shown in Figure 3, if the next data is transmitted from the transmitter at the time point t_3 , at which the busy signal S_2 and the acknowledge signal S_3 change to logic LOW, it is required a predetermined time for the acknowledge signal S_3 to change to logic HIGH, which may cause mis-operation of the CPU 10 because the data processing should be made whilst the acknowledge signal S_3 is still at the logic LOW state.

To reduce this problem, there is proposed a method of delaying the busy signal S_2 until the acknowledge signal S_3 changes to the logic HIGH at time point t_4 . In this case, however, there arises another problem that, in some cases, the so-called hand-shaking is executed by only the strobe signal S_1 and acknowledge signal S_3 . Furthermore, when the acknowledge signal S_3 is processed in the CPU 10 by the software, the acknowledge signal S_3 lasts at the logic LOW state for about $10\mu\text{sec}$ during which the CPU 10 only generates the acknowledge signal S_3 without processing other data. Therefore, the system performance is deteriorated overall.

Moreover, in the event that the busy signal S_2 and acknowledge signal S_3 are all dealt with in the software processing as illustrated in Figures 3 and 4, the output will be produced from one output port Y_0 and the other
5 output port Y_1 of the CPU 10, which may cause the CPU 10 to take a relatively long execution time. Such long execution time may be considered a negligible amount in some cases, however when it comes to a situation which should handle a great deal of data to be transmitted therethrough, the
10 system performance will be considerably influenced to a significant degree.

Accordingly, specific embodiments of the present invention aim to provide a circuit for controlling the
15 generation of a busy signal and an acknowledge signal properly to allow faster more accurate data communication between communication systems.

According to one aspect of the present invention a
20 control circuit, arranged to control the generation of an acknowledge signal and a busy signal in an interface is provided, the circuit comprising:

means for receiving a strobe signal;
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a busy signal generator arranged to generate a busy signal in response to said strobe signal and a busy signal generation control signal;

30 a central processing unit arranged to generate a processing completion signal;

an acknowledge signal generator arranged to generate an acknowledge signal dependent upon the condition of said
35 processing completion signal; and

means to provide control signals to said acknowledge
signal generator and to a busy signal generator, said
control signals being arranged to reset said busy signal
after a first predetermined time period has elapsed since
5 the generation of said processing completion signal, and
to reset said acknowledged signal after a second,
subsequent, predetermined time period has elapsed.

Preferably, said means to provide control signals to
10 said busy signal generator and said acknowledge signal
generator comprises a counter.

Preferably, said counter counts during said first
predetermined time period before providing a first control
15 signal to said busy signal generator and then counts
during said second predetermined time interval before
providing a second control signal to said acknowledge
signal generator.

20 Said first and second predetermined time periods are
preferably substantially equal.

Preferably, the circuit is arranged to control the
generation of an acknowledge signal and a busy signal in
25 a parallel interface.

According to a second aspect of the invention, a
control circuit arranged to control an acknowledge signal
and a busy signal in an interface, the circuit comprises:

30 an input from an interface unit, arranged to receive
data from a data communication device connected to said
interface unit and to receive an accompanying strobe
signal from said interface unit.

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a busy signal generator arranged to generate a busy signal in response to said strobe signal and a busy signal generation control signal;

5 a central processing unit arranged to control the entire circuit, the central processing unit being arranged to receive said busy signal and to generate a processing completion signal;

10 an acknowledge signal generator arranged to generate an acknowledge signal in response to the condition of said processing completion signal; and

a counter arranged to count a clock, in response to
15 said processing completion signal, which counter provides said acknowledge signal generator with an acknowledge signal generation control signal and provides a busy signal generator with said busy signal generation control signal;

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the arrangement being such that when data is received from said data communication device, together with the strobe signal from the interface unit, a busy signal is provided to the central processing unit from the busy
25 signal generator under the control of a busy signal generation control signal, the central processing unit being arranged to produce a processing completion signal when the received data has been processed, which processing completion signal is sent to the acknowledge
30 signal generator to provide an acknowledge signal to the interface unit and, substantially at the same time, to reset the counter which begins counting clock pulses, the busy signal generation control signal being reset after a predetermined time interval and the acknowledge signal

generation control signal being reset a predetermined time interval later.

5 Preferably, the switching is accomplished using a flip-flop which is clocked by the processing completion signal.

10 The invention includes an interface including a circuit substantially as herein described with reference to the accompanying drawings.

15 For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1 shows a conventional Centronics (RTM) compatible interface circuit;

20 Figure 2 shows a Centronics (RTM) compatible interface circuit; according to one embodiment of the present invention.

25 Figures 3 and 4 show waveforms of the control signals according to the conventional Centronics (RTM) compatible interface circuit of Figure 1; and

Figure 5 shows waveforms of the control signals according to the circuit of Figure 2.

30 Referring primarily to Figure 2, a circuit according to a preferred embodiment of the present invention, includes a Central Processing Unit (CPU) 10 for controlling the overall system, to which a busy signal generator 20 is coupled to provide an interrupt terminal

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INT of the CPU 10 with a busy signal S_2 generated therefrom. The busy signal generator 20 generates the busy signal S_2 to provide both the interrupt terminal INT of the CPU 10 and a busy terminal BUSY of a Centronics (RTM) interface cable 30 through a logic gate G_1 , under the control of a strobe signal S_1 produced from the Centronics (RTM) interface cable and an other predetermined control signal. The Centronics (RTM) interface cable 30 is designed to generate the strobe signal S_1 when data is received from another data communication device (not shown). In addition, an acknowledge signal generation control circuit 100 is coupled to the Centronics (RTM) interface cable 30 to control the generation of the acknowledge signal S_{32} provided to the Centronics (RTM) interface cable 30, under the control of the CPU 10. A control signal from the acknowledge signal generation control circuit 100 is coupled to a clear terminal of the busy signal generator 20 to control the generation of the busy signal S_2 .

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With respect to the construction of the acknowledge signal generation control circuit 100, a clock generator 60 generates a clock of a predetermined frequency and the clock signal is coupled to an input terminal of a logic AND gate G_3 , which produces a logic combination with a specific control signal from a D flip-flop 40 in response to the data processing completion signal S_{31} from the CPU 10. The output of the logic AND gate G_3 is applied to a counter 50 which counts the output of the gate G_3 to generate an acknowledge signal generation control signal S_8 and the busy release signal S_9 . Then, the output of an AND gate G_4 which logically combines the acknowledge signal generation control signal S_8 and a reset control signal $\overline{\text{RESET}}$, is coupled to a clear terminal $\overline{\text{CLR}}$ of the D flip-flop 40 which generates the acknowledge signal S_{32} .

synchronized with the terminal $\overline{\text{CLR}}$ of the busy signal generator 20 is coupled to the output of the AND gate G_2 , which logically combines the reset control signal $\overline{\text{RESET}}$ with the busy release signal S_9 .

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In operation, if data is received from the other data communication device, the strobe signal S_1 is generated and sent to the busy signal generator 20 from the Centronics (RTM) interface cable 30 at time point t_1 of Figure 5. At this moment, the busy signal S_2 of logic HIGH is generated from the busy signal generator 20 and applied to an input terminal of the OR gate G_1 and at the same time to the interrupt terminal INT of the CPU 10, thereby informing the other data communication device that the system is in the data receiving state.

When the CPU 10 completes the data processing by the interrupt signal (which hereinafter, for convenience, refers to the busy signal S_2 applied to the interrupt terminal INT of the CPU 10), then the data processing completion signal S_{31} is generated through the output port Y_1 which activates the acknowledge signal generation control circuit 100. The data processing completion signal sets the initial value of the counter 50 to zero. On the other hand, the D flip-flop 40 is clocked at the rising edge of the data processing to produce the logic HIGH state through an inverting terminal $\overline{Q}$ thereof to the acknowledge signal input terminal $\overline{\text{ACK}}$ of the Centronics (RTM) interface cable 30. The acknowledge signal of logic HIGH which is the output of the inverting terminal $\overline{Q}$ of the D flip-flop 40, is changed to the logic LOW state at time point t_2 of Figure 5.

At this moment, the CPU 10 completes the Centronics (RTM) hand-shaking operation and gets ready for receiving

the next data. After the time point t_9 , since the non-inverting output Q of the D flip-flop 40 which is applied to an input terminal of the AND gate G_1 is at the logic HIGH state as shown in Figure 5, the clock output CLKout of the clock generator 60 will be delivered to the clock input terminal CKin of the counter 50, at which the clock is counted, through the AND gate G_3 .

In this embodiment, the maximum counting value of the counter 50 is established to count about up to $10\mu\text{sec}$ by adjusting the clock generator 60. Therefore, if the counter reaches the maximum value, the acknowledge signal S_{32} is changed to the logic HIGH state at the time point t_{11} . In this case, the busy signal S_2 is changed to the logic LOW at the time point t_{10} at which the counter value is the half, i.e. $5\mu\text{sec}$, of the maximum counting value ($10\mu\text{sec}$). At this moment, the busy release signal S_1 from the counter 50 is provided to the busy signal generator 20 through the AND gate G_2 , releasing the busy state. Therefore, at the time point t_{10} , it is possible to receive the next data.

As stated heretofore, according to the present invention, since the CPU 10 controls the generation of the busy signal and acknowledge signal only by the acknowledge generation control signal, the system performance can be improved. Furthermore, unlike the conventional method, it is not required for the above described system to waste about $10\mu\text{sec}$ because the CPU 10 completes the generation of the acknowledge signal by one-time port accessing. It is another advantage of the above described embodiment of the present invention that even in the event that a communication system using a relatively low-speed CPU is used, a stable and accurate data communication is secured,

because the busy signal and acknowledge signal are generated by hardware, allocating enough time interval.

Although specific constructions and procedures of
5 the invention have been illustrated and described
herein, it is not intended that the invention be limited
to the elements and constructions disclosed. One skilled
in the art will easily recognize that the particular
elements or subconstructions may be used without departing
10 from the scope of the invention.



CLAIMS:

1. A control circuit, arranged to control the generation
of an acknowledge signal and a busy signal in an
5 interface, the circuit comprising:

means for receiving a strobe signal;

10 a busy signal generator arranged to generate a busy
signal in response to said strobe signal and a busy signal
generation control signal;

a central processing unit arranged to generate a
processing completion signal;

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an acknowledge signal generator arranged to generate
an acknowledge signal dependent upon the condition of said
processing completion signal; and

20 means to provide control signals to said acknowledge
signal generator and to a busy signal generator, said
control signals being arranged to reset said busy signal
after a first predetermined time period has elapsed since
the generation of said processing completion signal, and
25 to reset said acknowledged signal after a second,
subsequent, predetermined time period has elapsed.

2. A circuit according to Claim 2 or Claim 3 wherein
said means to provide control signals to said busy signal
30 generator and said acknowledge signal generator comprises
a counter.

3. A circuit according to Claim 2 wherein said counter
counts during said first predetermined time period before
35 providing a first control signal to said busy signal



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generator and then counts during said second predetermined time interval before providing a second control signal to said acknowledge signal generator.

5 4. A circuit according to Claim 3 wherein said first and second predetermined time periods are substantially equal.

10 5. A circuit according to any of the Claims 2 to 4 which is arranged to control the generation of an acknowledge signal and a busy signal in a parallel interface.

15 6. A control circuit arranged to control an acknowledge signal and a busy signal in an interface, the circuit comprising;

an input from an interface unit, arranged to receive data from a data communication device connected to said interface unit and to receive an accompanying strobe signal from said interface unit.

20 a busy signal generator arranged to generate a busy signal in response to said strobe signal and a busy signal generation control signal;

25 a central processing unit arranged to control the entire circuit, the central processing unit being arranged to receive said busy signal and to generate a processing completion signal;

30 an acknowledge signal generator arranged to generate an acknowledge signal in response to the condition of said processing completion signal; and

35 a counter arranged to count a clock, in response to said processing completion signal, which counter provides



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said acknowledge signal generator with an acknowledge signal generation control signal and provides a busy signal generator with said busy signal generation control signal;

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the arrangement being such that when data is received from said data communication device, together with the strobe signal from the interface unit, a busy signal is provided to the central processing unit from the busy
10 signal generator under the control of a busy signal generation control signal, the central processing unit being arranged to produce a processing completion signal when the received data has been processed, which processing completion signal is sent to the acknowledge
15 signal generator to provide an acknowledge signal to the interface unit and, substantially at the same time, to reset the counter which begins counting clock pulses, the busy signal generation control signal being reset after a predetermined time interval and the acknowledge signal
20 generation control signal being reset a predetermined time interval later.

7. A circuit according to Claim 6 wherein the switching is accomplished using a flip-flop which is clocked by the
25 processing completion signal.

8. A circuit substantially as herein described with reference to the accompanying drawings.

9. An interface including a circuit substantially as
30 herein described with reference to the accompanying drawings.

10. A method of controlling the generation of a busy
35 signal and an acknowledge signal in an interface, the



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method being substantially as herein described with
reference to the accompanying drawings.