

ABSTRACT**EMBEDDED MEMORY IN INTERCONNECT STACK ON SILICON DIE**

A method including forming a plurality of first interconnects and a plurality of second interconnects on opposite sides of an integrated circuit device layer including a plurality of circuit devices, wherein forming ones of the plurality of first interconnects and a plurality of second interconnects includes embedding memory devices therein. An apparatus including a substrate including a plurality of first interconnects and a plurality of second interconnects on opposite sides of an integrated circuit device layer including a plurality of circuit devices, wherein ones of the plurality of first interconnects and a plurality of second interconnects includes memory devices embedded therein.

Fig. 1