

Input circuits for intermediate- and high-frequency amplifiers in part possess an asymmetrical input and a symmetrical output. Input impedance values predominantly of between 50Ω and 300Ω are required, as used for terminating impedances of cables or filters. Generally further amplifier stages or selection means are connected to the output.

Fields of application for such input circuits are, for example, cable terminal amplifiers for wide-band transmission channels, antenna amplifiers and IF amplifiers with a low input impedance for matching to a preceding filter. A further, advantageous application consists in the initial amplification of the signals of light-sensitive diodes. In a conventional solution to the problem, bipolar transistors in a base- or grounded base circuit are used and frequently matching-transformers.

A solution more suitable for integration has been disclosed in German Patent 29 46 952. In the known circuit, in a differential stage composed of two bipolar transistors and a current source, a third transistor is connected to the interconnected emitters of the two transistors, and specifically by its emitter to the negative connection point of the current supply or earth, by its base to the emitters of the two transistors and by its collector to a working resistor which leads to the positive connection point of the current supply. Additionally, two resistors R_a , R_b are connected to the collector of the third transistor, which resistors lead to a respective input (A, B) of the differential stage, i.e. to the base of the first and second transistors respectively. In such a differential stage the potential of the inputs is fixed at approximately two forwards voltages via earth. If an input signal U_e is applied to the input A, the operating mechanism of this circuit leads to the occurrence of an inverted signal $-U_e$ at

the input B and the differential stage behaves as if it were symmetrically driven with $2 U_e$. Here half the value of the resistor R_a serves as input impedance. However, this applies only to not too high frequencies. If the transistor parameters become frequency-dependent, so also does the input impedance. In terms of frequency response the known circuit also has the disadvantage that it comprises an uncompensated reaction between the outputs of the differential stage and the inputs via the collector-base capacitor. The noise contribution of the third transistor also constitutes a disadvantage of the known circuit. Although this contribution disappears when the two inputs are connected in an identical fashion, normally this is not possible. The noise of the third transistor contributes to the unavoidable noise of the differential stage.

The aim of the invention is to provide an input circuit for high-frequency amplifiers, wherein the transistor parameters exhibit the least possible frequency dependence and wherein the reaction from the output to the input is as small as possible. This aim is fulfilled in an input circuit for high-frequency amplifiers according to the invention by the characterising features of Claim 1.

In the input circuit according to the invention, current requirement, noise and transmission characteristic correspond substantially to the properties of a simple differential stage. The input impedance is dependent upon the current flow and therefore can also be controlled or electronically adjusted. The frequency dependence of the input impedance is small and the circuit possesses a screening effect between input and output, thus enabling substantially higher frequencies to be transmitted than in the case of the known circuit.

The invention will now be explained in detail in the form of exemplary embodiments making reference to a drawing wherein:

Fig. 1 illustrates an arrangement according to German Patent 29 46 952;

Fig. 2 illustrates an input circuit according to the invention with a symmetrical output;

Fig. 3 illustrates a typical transmission characteristic of this input circuit;

Fig. 4 illustrates an input circuit with controllable input impedance and following differential amplifier;

Fig. 5 illustrates an input circuit with asymmetrical output;

Fig. 6 illustrates an input circuit with base current compensation.

The circuit according to German Patent 29 46 952 shown in Figure 1 consists of the differential stage with the transistors T1 and T2, the current source I_0 and the two working resistors R3 and R4. The main effect of this circuit is produced by the transistor T3, the emitter of which is connected to earth, the base of which is connected to the connection point of the emitters of the transistors T1, T2, and the collector of which is connected via the working resistor R5 to the supply voltage U_B . The resistors R1, R2 connect the collector of the third transistor T3 to the input terminals A, B of the differential stage, where R2 can also be 0. The transistor T3 is provided with negative feedback via the transistors T1, T2 of the differential stage, which in this case act as emitter followers. The operating point of the transistor T3 is adjusted by R5 in accordance with the current.

The potential of the input terminals A, B is thus fixed. If the input A is supplied with a voltage change U_e , a change of approximately $-U_e$ occurs at the input B. As thus $2 U_e$

falls across R_1 , the input impedance at terminal A becomes approximately $R_1/2$. On the one hand this is an advantage of this known arrangement since the input impedance required in accordance with high-frequency technology is produced in floating fashion and no further measures are required for supplying the second input B of the differential stage. On the other hand, by virtue of the active generation of the input impedance $R_1/2$ at the input A with the cooperation of three transistors a relatively limited frequency range results. In an integrated design there is also no simple means of correcting temperature dependence and scattering of the resistance R_1 . For an application at relatively higher frequencies, at approximately 10.7 MHz, the reaction from the outputs C, D upon the inputs A, B is also a disadvantage, for the suppression of which additional measures are generally required. Finally the noise contribution made by the third transistor to the overall noise is not small and impairs the function of pre-amplifier.

Figure 2 illustrates an exemplary embodiment of the circuit according to the invention. The circuit according to Figure 2 comprises four transistors T1 ... T4 of the same conductivity type. It is described by the following list of connections:

Emitter T1 - emitter T2 - earth (reference node);

Input A - base T1 - resistor R_1 (can be 0);

Collector T1 - emitter T3 - resistor R_1 - base T2;

Collector T2 - emitter T4;

Base T3 - base T4 - resistor R_3 - resistor R_4 (one of the two can be 0);

Collector T3 - resistor R3 - current source I3 - output C;

Collector T4 - resistor R4 - current source I4 - output D.

The signal source Qs, which is represented by a voltage source U_s and the internal resistance R_s , is connected via a coupling capacitor C_k .

To describe the operating mechanism in simplified form, the base currents can initially be ignored. It will also be assumed that $I_3 = I_4$ and $R_3 = R_4$. In the rest state no voltage then falls across R_1 and the two transistors T1, T2 have the same operating point. The operating current of all the transistors is identical. A signal current I_s generates a voltage drop $R_1 I_s$ across the resistor R_1 , which is simultaneously the difference between the two base voltages of the first and second transistors T1, T2. The first and second transistors T1, T2 are supplied with the sum current $I_3 + I_4 + I_s$. This total current is divided between the first and second transistors and forwarded into the transistors T3, T4, where the signal current I_s is subtracted again in the first transistor. The division can be calculated with the aid of the equation of the ideal transistor

$$I_c = I_{co} (e^{U_{BE}/U_T} - 1)$$

wherein I_{co} is the transfer residual current and $U_T = kT/q$ is the temperature voltage. Then an output voltage between the output terminals C, D of

$$U_{CD} = (R_3 + R_4) \frac{I_3 + I_s - a I_4}{1 + a}$$

results, where $a = e^{I_s R_1 / U_T}$.

Fig. 3 shows the dependence of the output voltage U_{CD} upon I_S for $I_3 = I_4 = 100 \mu A$, $R_1 = 5 k\Omega$, $R_3 = R_4 = 5 k\Omega$, $U_T = 26 mV$ ($300^\circ K$). Except for a slight asymmetry caused by the element I_S in the numerator of the formula, the equation is identical to that of the circuit according to Fig. 1. By linearisation in the vicinity of $I_S = 0$, where $I_g = I_3 + I_4$ and $R_g = R_3 + R_4$

the transfer impedance

$$\frac{U_{CD}}{I_S} = \frac{1}{4} \left(2 - I_g \frac{R_1}{U_T} \right) R_g$$

the voltage amplification

$$\frac{U_{CD}}{\Delta U_A} = \frac{I_g R_g}{2 U_T} \frac{2 U_T - I_g R_1}{2 U_T + I_g R_1}$$

and the input impedance

$$R_e = \frac{2 U_T}{I_g} + \frac{R_1}{2}$$

are obtained.

The cases wherein $R_1 = 0$ and $R_1 \gg 2 U_T/I_g$ are of particular interest. The case in which $R_1 = 0$ is illustrated in Fig. 4. The input impedance is then $R_e = 2 U_T/I_g$ and can be easily influenced by the adjustment or control of I_g' . For this purpose a current mirror circuit with the transistors T_8 , T_9 and T_{10} is provided which converts the current I_g' into the two currents I_3 , I_4 . In order for example to produce an input impedance of 75Ω , a current $I_3 + I_4 = 2 U_T/R_e = 0.33 mA$ at room temperature is required. This shows that even low input impedances can be attained with a low current drain. The value of the voltage amplification nevertheless corresponds to that of the simple differential stage or the circuit according to Fig. 1. Here the highest cut-off frequency is also achieved. The situation in which $R_1 \gg 2 U_T/I_g$ is illustrated in Fig. 2 and Fig. 5. The input impedance approximates $R_1/2$ as in the known circuit according to Fig. 1. The voltage amplification has almost the same value as previously, but with the reverse sign. The transfer impedance increases with R_1 and likewise has a reverse sign. The attainable cut-off frequency falls compared to the case in which $R_1 = 0$, but is still

substantially higher than in the arrangement according to Fig. 1.

A further advantage of the arrangement according to the invention consists in that the voltage of the two interconnected bases of the third and fourth transistors T3, T4 relative to the reference node M is not dependent upon the signal. Only in the event of overdriving does a reduction occur in this voltage. Thus the circuit cannot be disturbed by capacitive effects from the bases of the two transistors T3, T4. In particular, as in a cascade stage, the input circuit is screened from the outputs C, D.

With regard to the noise behaviour it should be noted that the two transistors T3, T4 do not make a substantial noise contribution as they only pass on, and do not control, the current. The noise of the first and second transistors T1, T2 is equivalent, however, to the noise of a corresponding differential stage. Thus a better noise behaviour is achieved for the solution according to the invention compared to the arrangement shown in Fig. 1.

In an arrangement according to Fig. 4 the electrical symmetry is somewhat disturbed by the fact that the base currents of the first and second transistors T1, T2 are conducted across the transistor T3, while the other path with the transistor T4 remains unloaded. This leads to a faulty d.c. voltage between the output terminals C, D. If this is disturbing, compensation can be effected with a simulation transistor T5, which is supplied via a further transistor T11 of the current mirror.

For this purpose two resistors R5, R6 are connected to the collector of the transistor T5, where the resistor R5 is connected to the base of T5 and the resistor R6 is connected

to the input terminal. The desired compensation is achieved if approximately $R_6 = R_5/2$ is selected.

Another possibility of base current compensation is shown in Fig. 6. Here a transistor T12 is connected by its emitter to the connection point of the two bases of the transistors T3, T4 and by its base to the connection point E of the two resistors R3, R4, while the collector of the transistor T12 is connected to the input of a current mirror composed of the transistors T13 and T14. The output of the current mirror, which is formed by the collector of the transistor T14, is connected to the input terminal A. In this way the base current of the transistors T3, T4, which is very similar to the base current of the transistors T1, T2, is taken up by the transistor T12 and supplied to the circuit input via the current mirror T13, T14. Here no additional current is required as in the arrangement shown in Fig. 4. It can also be advantageous that the potential of the outputs C, D exceeds the potential of the bases of the transistors T3, T4 by the base-emitter voltage of the transistor T12, thereby facilitating a greater voltage range at the outputs C, D of the arrangement.

The insertion of the resistor R1 according to Fig. 2 or Fig. 5 improves the asymmetry of the currents through the transistors T3, T4 since the voltage drop across R1 reduces the base-emitter voltage of the transistor T1 and thus reduces its collector current. In the case of a relatively larger resistance R1, however, over-compensation occurs. To avoid this effect it is also provided that the base of the second transistor T2 be preceded by a resistor R2, as illustrated in Fig. 5.

The circuit according to Fig. 6 permits the outputs C, D to be driven more strongly because the collectors of the transistors T3, T4 carry a higher potential than the

interconnected bases. If this property is required and it is possible to dispense with base current compensation, the transistors T13, T14 can be omitted and the collector of the transistor T12 can be connected to the supply voltage UB. It is also possible to insert one or more diodes and/or a resistor between the connection point E of the resistors R3, R4 and the base of the transistors T3, T4.

In most applications a symmetrical output with $I_3 = I_4$ and $R_3 = R_4$ will be required, as shown in the example according to Fig. 4 with coupling of a differential stage. Depending upon the ratio I_3/I_4 and R_3/R_4 , asymmetrical drive- and potential conditions can also be set up. Fig. 5 illustrates an example in which $I_4 = 0$ and $R_4 = 0$, where the entire supply current I_0 is supplied on one side and the transistor T4 operates only as diode. The amplified signal then appears on one side at the output C, while only a rest potential occurs at the output D.

Claims

1. An input circuit for high-frequency amplifiers with four transistors of the same conductivity type, characterised in that the emitters of the first and second transistors (T1, T2) are connected to a reference point (M), that the base of the first transistor (T1) forms the input (A) of the circuit, that the base of the second transistor (T2) is connected to the collector of the first transistor (T1), that the collector of the first transistor (T1) is connected to the emitter of the third transistor (T3) and the collector of the second transistor (T2) is connected to the emitter of the fourth transistor (T4), that the bases of the third and fourth transistors (T3, T4) are connected to one another and that at least one of the collectors of the third or fourth transistor (T3, T4) is connected to a current supply (I3, I4).
2. An input circuit as claimed in Claim 1, characterised in that the base and the collector of the first transistor (T1) are connected to one another.
3. An input circuit as claimed in Claim 1, characterised in that a resistor (R1) is connected between the base and the collector of the first transistor (T1).
4. An input circuit as claimed in one of Claims 1 to 3, characterised in that the collector of the third transistor (T3) is connected to the base of the third transistor (T3) and the collector of the fourth transistor (T4) is connected to the base of the fourth transistor (T4), where at least one connection takes place via a resistor (R3, R4).
5. An input circuit as claimed in one of Claims 1 to 3, characterised in that the collectors of the third and fourth



transistors (T3, T4) are connected to a node (E), where at least one connection takes place via a resistor (R3, R4), and that the node (E) is connected via a further impedance, for example the base-emitter path of a transistor (T12), to the bases of the third and fourth transistors (T3, T4).

6. An input circuit as claimed in one of Claims 1 to 5, characterised in that a resistor (R2) is connected in series with the base of the second transistor (T2).

7. An input circuit as claimed in one of Claims 1 to 6, characterised in that at least one of the bases of the first and second transistors (T1, T2) is supplied with a current which corresponds approximately to the base current.

