

Description

Field of Invention

5 The present invention relates to the field of power regulation. More particularly, the invention relates to a regulator useful in apparatus intended to receive electrical power from an external, alternating magnetic field. Most particularly the invention relates to a regulator adapted for substantially total integration on a single VLSI "chip".

10 Examples of practical devices falling into the above categories would include baggage identification tags, personnel security badges, electronic locks and keys, remote-controlled actuators, and "smart" credit cards.

Prior Art

15 In apparatus adapted to receive power from an external magnetic field, a particular problem has been to compensate for variations in the field intensity at different points in space. This causes the apparatus to receive variable amounts of electrical power.

For such applications, the so-called "shunt" regulator configuration is usually preferred, for the following reasons:

20 a) The shunt regulator possesses inherent ability to control its input voltage. Regulators such as the "series" type can control only their output, while the input voltage may rise to dangerous levels. The series-type regulators are therefore not desirable when the regulator is to be included with the remainder of the required circuitry, on a single VLSI "chip", as such chips are highly susceptible to damage by over-voltages. The shunt regulator by comparison, operates by imposing an additional load on its power source, sufficient to prevent the input voltage from rising above the intended value.

25 b) When the power available is only just sufficient to permit operation of the device, it is desirable that the regulator circuit itself should consume a minimum of additional power. Series regulators generally consume significant amounts of power in their own operation, while a shunt regulator may consume almost no power, as the shunt element ("L" in Fig. 1) is essentially turned off.

Several prior-art shunt regulators have been disclosed.

30 US 4,614,906 discloses the use of a shunt regulator to permit a plurality of loads to be connected across a single, high-voltage supply.

US 4,103,219 discloses a DC supply, rather than a resonant, AC supply. Essentially it follows the known configuration of Figure 1.

US 3,551,745 discloses the addition of an over-voltage trip to a conventional shunt regulator.

35 US 3,229,185 discloses an AC supply, although no resonant (it is a conventional transformer). It discloses means of improving the performance of the well-known Zener diode type of shunt regulator.

US 3,141,124 discloses additional loads switched into a (untuned) transformer circuit by Silicon Controlled Rectifier devices. These latter regulators are unsuitable for implementation in VLSI chips.

The principal elements of a shunt regulator, according to prior art, are shown in Figure 1.

40 The known shunt regulator consists of a DC power source, S, of uncertain voltage, connected through a resistance R, to output terminals, O, at which there is provided a stabilised voltage. The output voltage is sensed by the amplifier A, and compared to a known reference voltage, v, (developed by a zener diode, band-gap circuit, or the like). The amplifier develops an error voltage, proportional to the difference between the output and reference voltages. This error voltage serves to control the load L (which may take the form of a large transistor, or other power-absorbing device).

45 It can be seen that the current passing through R will be the sum of that delivered to the load at O, plus that drawn by the controlled load L. The controlling action is provided by adjusting the current through L so as to cause a voltage drop across R. This reduces the incoming voltage S to the desired output voltage, D.

50 Either the Output or Reference voltages may be attenuated by a resistive voltage divider circuit, before reaching the amplifier A, if desired.

It is apparent from the figure that all parts of the circuit, except the input resistor R, are subjected to the output voltage D, rather than the (higher) input voltage S. Hence, the shunt regulator serves to protect its input circuitry from over-voltages.

55 As can be seen, the prior art regulators do not readily lend themselves to integratability due to the use of large chip area consuming components such as the resistor, R.

A further disadvantage of certain prior art shunt regulators is apparent from consideration of Figure 2, which shows a regulator according to Figure 1, now modified to accept power from a resonant source LC. It will be apparent that the rectifier D is required to carry not only the "useful" current (ie that ultimately delivered

to the load at O) but also the "waste" power dissipated in the regulator load L. Thus the rectifier must be made larger than otherwise necessary. Similarly, the reservoir capacitor C must be increased in size, to contain the output - voltage "ripple" due to the additional current drawn by the shunt regulator.

As noted above, the present invention is concerned particularly, though not necessarily exclusively, with power supply circuits on physically isolated units such as baggage identification tags, personnel security badges, electronic locks and keys, remote-controlled actuators, and "smart" credit cards. The powering of such units by some form of inductive coupling is of course well known, as shown for example by US 4 650 981 and WO 87/06747.

The general object of the present invention is to provide an improved regulator circuit.

Accordingly the present invention provides power supply circuitry for rectifying and regulating an AC power supply (S), comprising a shunt circuit (L) and control means (A,V) for controlling the shunt circuit, characterized in that the shunt circuit (L, Figure 3; MREG, Figure 4) is connected across the AC source on the AC side of the rectifying means (D, Figure 3; M1-M3, Figure 4)).

Further preferred features of the invention will become apparent from the following detailed description and the claims.

Preferred embodiments of the present invention will now be described with reference to the accompanying drawings, wherein:

Figures 1 and 2 show prior art arrangements, and

Figures 3 and 4 show preferred embodiments of the present invention.

It should be noted that for simplicity the present disclosure is made with reference to a "negative ground" configuration. As would be understood by the skilled addressee, a "positive ground" configuration is equally possible, by reversing component polarities, and is to be understood as falling within the scope of the present invention. Likewise the present disclosure is made with reference to a CMOS implementation, while other forms (such as NMOS, bipolar, etc.) are also feasible, as would be appreciated by those skilled in the art.

Figure 2 shows a regulator configuration which has dispensed with resistor R.

The combination of two, known, circuits (the resonant power pick-up circuit and the shunt regulator) are seen to yield a circuit inherently protected against over-voltages. The elimination of the large resistor R is a further advantage.

With reference to Figure 2, as compared to Figure 1, the original DC power source has been replaced by a tuned capacitor power pick-up circuit LC for receiving an impinging magnetic powering field with a rectifier D and reservoir capacitor C. A well-known half-wave rectifier circuit is shown, however any standard rectifier configuration may be used.

The omitted resistor R has had its place taken by the tuned circuit LC, which is very loosely coupled to the AC power source (probably being some significant distance from it). In this situation, the voltage developed across LC will be that induced by the imposed magnetic field, multiplied by the "Q"-factor of the LC circuit. This "Q"-factor is highly dependent on the load applied to the LC circuit.

The function of the arrangement shown in Figure 2 may be considered by realising that the impinging magnetic field will deliver a certain amount of energy to the circuit LC, in each AC cycle. The voltage of the tuned circuit will therefore rise, until an equal amount of energy is removed, in each cycle, by the combined loads at L and C. The adjustable load L may therefore act to control the supply voltage in a manner similar to the circuit of Figure 1.

Conveniently, the tuned source LC will be designed according to the following criteria:

- a) It should be resonant at the desired operating frequency.
- b) It should be designed for substantially optimum power transfer (ie an "impedance match") to the useful load O, in the absence of the regulating element L. This condition may be recognised by comparing the "Q-factor" of the circuit LC alone (the "unloaded Q") with the "Q-factor" in the presence of the useful load O (the "loaded Q"). With optimal matching, the loaded Q will be half the unloaded Q.

If the above criteria is met, it has been found that the regulating action occurs by a combination of 3 mechanisms, in cooperation:

- a) excess energy is diverted into the load L
- b) the Q-factor of LC is reduced, so lowering the voltage seen
- c) the power-match to the load O is progressively reduced from optimum, so that less power is transferred to O.

The combination of these effects has the result that, as input power (ie magnetic field strength) is increased, power dissipation in the load L rises to a maximum, and then reduces. By contrast, the dissipation in a conventional shunt regulator will increase continually as the input field strength increases, thereby causing possible overheating problems.

It has been observed that in the arrangement of Figure 2, the rectifier D will conduct during only a small

portion (the 'conduction angle') of the entire AC cycle. The width of this conduction angle will depend on the value of the reservoir capacitor C, and on the total load current. Since the requisite total energy per cycle must still be delivered, the smaller the angle, the greater the peak current through the rectifier D.

5 If the load L is to absorb energy throughout the AC cycle, additional current must be supplied (during that portion of the AC cycle when the rectifier does not conduct) by the charge remaining on the capacitor C. Hence the voltage at C will fall by an excessive amount before C is charged again on the next cycle. The effect is to increase both the conduction angle and the output-voltage 'ripple'.

10 If, however, the amplifier is adapted to 'turn on' the load L only while the rectifier is conducting, excessive load on the capacitor C may be avoided but at the expense of a short 'conduction' angle, for L. As with the rectifier, this translates into high peak currents in L, and the need for a larger device to handle them. Further, the rectifier D must be of a size sufficient to carry not only the "useful" output current to O, but also the worst-case additional load through the regulator L. This can cause a considerable size increase when realising the device.

15 Figure 3 shows a regulator (an improvement on Figure 2) wherein the current paths used for voltage regulation (through L), and for useful output (through D and C) are separated. The use of a transistor (especially a MOS transistor) directly connected across the tuned circuit has been shown to confer significant benefits in the operation of such a shunt regulator, permitting the voltage regulating and power-delivery functions to be separated, with consequent size reductions to both groups of components. This yields especial benefits if the device is to be implemented in a VLSI assembly.

20 In the schematic, shown in Figure 3, the load L is shown as a P-channel MOS transistor, to demonstrate the particular suitability of this circuit for VLSI implementation. However, a bipolar transistor or other suitable device would also serve.

25 Circuit operation is as follows - The gate of L is biased to some value between GND and V+ (by a similar amplifier arrangement to that of Figure 2). When AC signal swings negative from GND, the transistor's gate is more positive than its channel, and no current flows. When the "AC" end of the transistor's channel swings above the gate voltage, the transistor begins to conduct. Since the AC signal exhibits a sinusoidal voltage about GND, the higher the gate voltage, the shorter the period ('conduction angle') during which the AC signal is above the gate voltage, and L conducts. Furthermore, the AC point rises to a lesser voltage above the gate, thus causing L to conduct less heavily.

30 The transistor therefore constitutes an adjustable load, as desired. It operates, as before, by loading the tuned circuit. It is to be noted that the resonant nature of the supply circuit LC, ensures that the waveform at AC remains substantially sinusoidal, in the presence of the intermittent loads presented by L and D.

35 It is apparent that not only does the current through L bypass, and accordingly not load, the rectifier D or the capacitor C, but also that the conduction angle of the load L may be varied at will, independently of that of the rectifier D. The components D and C may therefore be designed solely to handle the "useful load" delivered at O, while the transistor L is designed independently, to absorb sufficient power to exert adequate control.

40 Since the conduction angle at L may be increased to almost 180°, to achieve maximum loading, the peak current through L may be limited to a relatively modest value. This permits a reasonably sized transistor to be used at L.

It is possible to replace the single transistor L, by a parallel pair of transistors, of complementary polarities. In this case, the two transistors will conduct on opposite half-cycles of the AC waveform, and the total conduction angle can approach 360°.

45 Alternatively, the device hereinafter described may be employed to increase the conduction angle of a single transistor beyond 180 degrees.

An alternative embodiment of the present invention will now be described, with reference to Figure 4, which shows an embodiment designed for an application as follows:

Powering frequency: 132kHz
Required Output: 5V at 5mA

50 Figure 4 shows a complete power supply stage, including a Synchronous Rectifier, the subject of a co-pending Application, entitled "Integratable Synchronous Rectifier", filed 19th November, 1987 by the present applicant as Australian Provisional Patent Application No. PI 5507. Detailed circuit forms, appropriate to a 3-micron CMOS process, are given in the PSPICE file as hereinafter described. (PSPICE, an industry standard circuit simulation program, is published by MicroSim Corporation, USA).

55 In the example, a further design aim was to eliminate the usual, large DC output capacitor. The example circuit is capable with only the small reservoir capacitor CRES, of stabilising its output voltage, within 1V of target, and of correcting within 100uS, for input-voltage changes of 2:1, and for load resistance changes of 3:1.

The circuit configuration of Figure 4 is derived from that of Figure 3, with the following changes:

a) A Synchronous Rectifier (the subject of the copending Application) has been included, said Rectifier being placed in the negative supply rail, rather than (as in Figure 3) in the positive rail.

b) The error amplifier has been embodied as a voltage comparator and a SCF.

c) The circuit has been arranged so that all MOS transistors used in the power-processing circuits are of a single polarity (here, N-channel). This permits the VLSI chip to be laid out with no "well" boundaries near the power circuits, thereby conferring enhanced resistance to "latch-up", in view of the need to drive circuit nodes outside the power-supply rail voltages. N-channel transistors may be preferred for the power-processing circuits, due to their higher carrier mobility, which results in a N-channel device being typically 3 times smaller than a P-channel transistor designed for similar duty.

Circuit operation will be described, with reference to Figure 4. VIN represents the voltage induced in the coil L1 by the external AC magnetic field. RLS represents the ohmic losses associated with L1. C1 is the tuning capacitor.

X3, M1, M2, and M3 represent a Synchronous Rectifier, whose operation is described in the copending Application PI 5507.

The shunt load (L in Figure 3) is the transistor MREG, which conducts during those portions of the AC cycle when its Source is at a more negative voltage than its Gate. Since the said Source follows the AC wave, while the Gate is held at a substantially constant value, an adjustment of the Gate voltage will serve to vary the portion of the AC wave during which MREG conducts. In the example, this voltage is developed by the SCF comprising the pass-gates MF1, MF2, MF3, and the capacitors CIN, CLAG, CLEAD. This circuit serves to integrate the digital pulses from the comparator X4, which compares the output voltage with a 2.5V reference (assumed to be obtained from a Band-Gap, or other standard circuit). It may be noted that circuit economy is obtained by utilising the clock signal already developed for the Synchronous Rectifier to operate the SCF, via the BOOST block. The latter is a conventional non-overlapping 2-phase clock generator, whose output stages are arranged to develop voltages above the positive supply rail, thereby enabling the transmission gates MF1, etc., to transfer voltages approaching the full rail value.

The SCF is a conventional 3-component arrangement, in which CIN simulates a resistor, and provides a basic integration function with CLAG. CLEAD simulates a second resistor, and introduces a small phase-advance into the filter characteristic, which speeds up the circuit's response to disturbances.

Note particularly the division of CLEAD into two parts, as shown. In practice, CLEAD1 is partially embodied in the stray gate/channel capacitance of MREG, and additional capacitors are used to adjust the values of CLEAD1 and CLEAD2. With the driving clocks phased as shown, the switch MF2 is closed during the bulk of the AC cycle, while the switches MF1, MF3 are closed only briefly, during the conduction period of the Synchronous Rectifier. Observe further, that during such conduction period, the Source of MREG is substantially at zero volts (being connected to the negative rail via the Synchronous Rectifier). During this brief period, the charges on CLAG and CLEAD equilibrate, while CIN assumes either zero or a maximal value, according to the state of the comparator X4. As the Synchronous Rectifier ceases conduction, the charges on CIN and CLEAD equilibrate, while CLAG is isolated. As the AC cycle proceeds, the Source of MREG swings positive (attaining a maximum value of substantially twice the positive rail). Since part of CLEAD is returned to that Source, it follows that the Gate of CLEAD receives an additional positive charge, tending to keep MREG in conduction longer than would be the case were CLEAD returned entirely to the negative rail. This device increases the fraction of the AC cycle during which MREG can conduct, so increasing the energy which the regulator can remove from the tuned circuit. This permits a small transistor to be used at MREG, for a given regulating action.

The following text is an implementation of the embodiment shown in Figure 4 for PSPICE.

Resonant, Regulated Supply [SUPPLY4.CIR]

* Mk-IV Version, using SCF and boosted NMOS clocks in
Regulator loop

5 * Test for Line Regulation

*

.option itl5=0 limpts=1000

10 + reltol=1e-4 ;Reduced RELTOL for high-Q ckts.

*

.Lib..\3micron.lib ;Semiconductor library file

* (MOS Device Models)

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*
.SUBCKT synrect 10 11 12 13 ;The Synchronous Rectifier
5  *
    proper
* Nodes are:      10      11      12      13
*      +ve Rail  Ac Input Switch-Input Driver
*
10 m1 11 13  0  0 ntarg w=1800u l=5u ;The actual rectifying
    *      switch
    *      Longer, to take high
    *      voltages
15 m2 13 12  0  0 ntarg w=12u l=3u ;The driving Buffer
    m3 10 12 13 10 ptarg w=36u l=3u ;P-channel wider, to even
    *      drive
20 .ENDS
    *
    *
.SUBCKT comparator 10 11 12 13 ;Voltage Comparator
25 * Nodes are:      10      11      12      13
    *      +ve Rail  Non-Inv In  Output  Invt In
    *
    *      The "real" comparator
30 * m1 10 15 14 10 ptarg w=3u l=5u ;First Input
    * m2 14 11  0 10 ptarg w=3u l=8u
    * m3 10 15 15 10 ptarg w=3u l=5u ;Second Input
35 * m4 15 13  0 10 ptarg w=3u l=8u
    * m5 10 15 17 10 ptarg w=11u l=8u ;Current Source
    * m6 17 14 16 10 ptarg w=22u l=4u ;The Balanced Pair
    * m7 17 15 12 10 ptarg w=22u l=4u
40 * m8 16 16  0  0 ntarg w=6u l=15u ;Output Stage
    * m9 12 16  0  0 ntarg w=6u l=15u ; (Current Mirror)
    *
    *      For faster simulation: quickie comp.
45 rser 11 13 1e9 ;So no floating nodes
    s1  10 12 13 11 compsw ;Simulate from
    ; controlled switches
50 s2  12  0 11 13 compsw
    .model compsw vswitch(ron=1e4 roff=1e9 von=-0.01 voff=0.01)
    .ENDS

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*
***** NMOS Clock Booster - non overlapping pair
5 *           Fast, "dummy" hot-clock source
*           See BOOST.CIR for the full circuit
*
10 .model topsw vswitch (ron=1e4 roff=1e9 von=0.1 voff=1.0)
    .model botsw vswitch (ron=1e4 roff=1e9 von=-1.0 voff=-0.1)
*
    .subckt side 20 21 22 24 25           ;Half the driver
15 esense      23 22 20 21 1.0           ;Transfer the input
*                                       voltage
    rload      23 0      1e9             ;No floating nodes
    stop       24 25 23 0 topsw          ;Output switches
20 sbottom     25 0 0 23 botsw
    cout       25 0      100ff           ;Finite switching time
    .ends
    *SUBCKT boost 1 10 12 13             ;Vdd - IN - Out+ - Out-
25 *
    eboost 2 0 1 0 1.4                   ;Develop the "hot-clock"
*                                       voltage
*
30 x1 1 10 13 2 12 side                   ;The driver proper
    x2 10 0 12 2 13 side
*
35 .ENDS
*
***** The Full Regulator Circuit *****
*
40 *                                       ;The primary AC source
    vin 1 34 ac 2.0 132khz
    +      sin(0 2.0 132khz)             ;Induced AC voltage
    vst 34 32 sin(0 -1.0 132khz 227.28uS) ;Step in Input ampl.
45 *
    l1 32 33 48.5uH                      ;The main resonant
*                                       components
50 rls 33 2 1.7                          ; and their losses
    c1 1 2 30nF
    rcp 1 2 6200

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*
*
5  x2  1  2  3 15 synrect          ;Synchronous rectifier
   x3  1  2  3  0 comparator      ;Rectifier Driver
   ***** The SCF Regulator Filter *****
10  * NB While AC swings high, the 2 caps. are paralleled, so
   * minimising over-voltage effects due to charge-pumping from
   * MREG's channel
   *
15  mreg 1 14  2  0 ntarg w=3000u 1=3u ;The shunt regulator *
      proper
      It carries only Vdd
      (each dirn.)
20  *
   x20  1 15 17 18 boost          ;S.C.F. Clock Driver
   mf1 12 17 13  0 ntarg          ;SCF switch no. 1
   mf2 13 18 14  0 ntarg          ;
25  mf3 14 17 16  0 ntarg          ;
   cin      13  0 5.0pF          ;Input capacitor
   *clead   14  0 2.0pF          ;Phase-advance, with Cgs of
   *                          Shunt trans.
30  clag      16  0 10pF          ;The main phase-lag
   *
   *                          Shunt Regulator
35  x4  1 10 12 11 comparator      ;Test Voltage
   vref  11  0 dc 2.5V            ;Voltage Reference
   rtop  1 10      1Meg           ;Feedback Sense
   rbot  0 10      1Meg
40  *
   rl  1  0      1000             ;Useful load - 25mW at 5V
   cres 1  0      56nF            ;Output reservoir cap.
   *
45  ***** Test to be Run *****
   .probe v(1) v(2) id(mreg) i(vin) v(32)
   +   v(12) v(13) v(14) v(15) v(16) v(17) v(18)
50  .tran lus 350us
   .end

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NMOS Clock Booster - non-overlapping pair [BOOST.CIR]
Vdd 1 0 5
5 Vin 10 0 pulse(0 5 10n 2n 2n 60n 140n)
  .Lib 3micron.lib
  .tran 10n 200n
  .probe
10 *
  .subckt biginv 1 2 3      ;Wide Inverter
  m1 1 2 3 1 ptarg w=15u
  m2 0 2 3 0 ntarg w=5u
15 .ends
  *
  .subckt smlinv 1 2 3      ;Small Inverter
20 m1 1 2 3 1 ptarg
  m2 0 2 3 0 ntarg
  cd 0 3 100ff              ;Short delay
  .ends
25 *
  .subckt driver 1 2 8      ;The High-Voltage Clock Driver
  *                          (inverting)
30 x1 1 2 3 biginv          ;The delay chain
  x2 1 2 4 smlinv           ;The delay allows CB to charge,
  *                          before boost
  x3 1 4 5 smlinv
35 x4 1 5 6 smlinv
  x5 1 6 7 biginv
  md 3 1 8 0 ntarg w=20u    ;Output "diode"
  cb 7 8 300ff              ;Boost cap.
40 .ends
  *
  .subckt norgate 1 2 3 4    ;2-input NOR gate
45 m1 1 2 5 1 ptarg
  m2 5 3 4 1 ptarg
  m3 4 2 0 0 ntarg
  m4 4 3 0 0 ntarg
50 .ends

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55

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*
x10 1 10 11      smlinv      ;The Mead/Conway clock circuit
x11 1 11 13 14 norgate
5 x12 1 10 12 15 norgate
x13 1 14 16      smlinv
x14 1 15 17      smlinv
10 x15 1 16 12      driver
x16 1 17 13      driver
*
m11 1 12 21 0 nslow l=5u w=5u ;Dummy loads
15 m12 1 13 22 0 nslow l=5u w=5u
r11 0 21 1e7
r12 0 22 1e7      ;Show how high a pass transistor
20 *                can pull
.end

```

25 Claims

1. Power supply circuitry for rectifying and regulating an AC power supply (S), comprising a shunt circuit (L) and control means (A,V) for controlling the shunt circuit, characterized in that the shunt circuit (L, Figure 3; MREG, Figure 4) is connected across the AC source on the AC side of the rectifying means (D, Figure 3; M1-M3, Figure 4)).
2. Power supply circuitry according to claim 1, characterised in that the rectifying means comprise diode means (D, Figure 3) and are coupled to charge storage means (C).
3. Power supply circuitry according to either previous claim, characterised in that the AC source comprises a resonant circuit (LC, Figure 3; L1-C1, Figure 4).
4. Power supply circuitry according to any previous claim, characterised in that the resonant circuit is inductive coupled to an AC power source.
5. Power supply circuitry according to either of claims 3 and 4, characterised in that the control means controls the apparent Q factor of the resonant circuit.
6. Power supply circuitry according to claim 5, characterised in that the shunt circuit comprises switching elements, whereby there is substantially no resistive power dissipation therein.
7. Power supply circuitry according to claim 6, characterised in that the shunt circuit comprises at least one MOS transistor (L, Figure 3; MREG, Figure 4).
8. Power supply circuitry according to claim 7, characterised in that the shunt circuit comprises a plurality of transistors all of the same polarity.
9. Power supply circuitry according to any previous claim, characterised in that the control means comprise a voltage comparator (X4, Figure 4) and a switched capacitor filter (MF1, MF2, MF3, CIN, CLAG, CLEAD1, CLEAD2).
10. Power supply circuitry according to claim 9, characterised in that the switched capacitor filter provides a drive signal to the shunt circuit through substantially the whole of the period of the AC waveform.

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*
x10 1 10 11    smlinv    ;The Mead/Conway clock circuit
x11 1 11 13 14 norgate
5 x12 1 10 12 15 norgate
x13 1 14 16    smlinv
x14 1 15 17    smlinv
10 x15 1 16 12    driver
x16 1 17 13    driver
*
m11 1 12 21    0 nslow l=5u w=5u ;Dummy loads
15 m12 1 13 22    0 nslow l=5u w=5u
r11 0 21 1e7
r12 0 22 1e7    ;Show how high a pass transistor
20 *              can pull
.end

```

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1. Power supply circuitry for rectifying and regulating an AC power supply (S), comprising a shunt circuit (L) and control means (A,V) for controlling the shunt circuit, characterized in that the shunt circuit (L, Figure 3; MREG, Figure 4) is connected across the AC source on the AC side of the rectifying means (D, Figure 3; M1-M3, Figure 4)).
2. Power supply circuitry according to claim 1, characterised in that the rectifying means comprise diode means (D, Figure 3) and are coupled to charge storage means (C).
3. Power supply circuitry according to either previous claim, characterised in that the AC source comprises a resonant circuit (LC, Figure 3; L1-C1, Figure 4).
4. Power supply circuitry according to any previous claim, characterised in that the resonant circuit is inductive coupled to an AC power source.
5. Power supply circuitry according to either of claims 3 and 4, characterised in that the control means controls the apparent Q factor of the resonant circuit.
6. Power supply circuitry according to claim 5, characterised in that the shunt circuit comprises switching elements, whereby there is substantially no resistive power dissipation therein.
7. Power supply circuitry according to claim 6, characterised in that the shunt circuit comprises at least one MOS transistor (L, Figure 3; MREG, Figure 4).
8. Power supply circuitry according to claim 7, characterised in that the shunt circuit comprises a plurality of transistors all of the same polarity.
9. Power supply circuitry according to any previous claim, characterised in that the control means comprise a voltage comparator (X4, Figure 4) and a switched capacitor filter (MF1, MF2, MF3, CIN, CLAG, CLEAD1, CLEAD2).
10. Power supply circuitry according to claim 9, characterised in that the switched capacitor filter provides a drive signal to the shunt circuit through substantially the whole of the period of the AC waveform.



11. Power supply circuitry according to either of claims 9 and 10, characterised in that the rectifier is a synchronous rectifier (X3, M1, M2, M3).
12. Power supply circuitry according to claim 11, characterised in that the switched capacitor filter and the synchronous rectifier are driven from a common clock signal.
13. Power supply circuitry according to any previous claim, characterised in that the circuit is integrated.

10 Patentansprüche

1. Stromversorgungsschaltkreis zur Gleichrichtung und Regelung einer Wechselstromquelle (S) mit einem Nebenschlußstromkreis (L) und einem Steuermittel (A, V) zur Steuerung des Nebenschlußstromkreises, dadurch gekennzeichnet, daß der Nebenschlußstromkreis an der Wechselstromseite des Gleichrichtermittels (D, Fig. 3; M1-M3, Fig. 4) der Wechselstromquelle parallel geschaltet ist.
2. Stromversorgungsschaltkreis nach Anspruch 1, dadurch gekennzeichnet, daß das Gleichrichtermittel Di-odenmittel (D, Fig. 3) aufweist und mit einem Ladungsspeichermittel (C) gekoppelt ist.
3. Stromversorgungsschaltkreis nach einem vorhergehenden Anspruch, dadurch gekennzeichnet, daß die Wechselstromquelle einen Resonanzkreis (LC, Fig. 3; L1-C1, Fig. 4) enthält.
4. Stromversorgungsschaltkreis nach irgendeinem vorhergehenden Anspruch, dadurch gekennzeichnet, daß der Resonanzkreis induktiv an eine Wechselstromquelle angekoppelt ist.
5. Stromversorgungsschaltkreis nach einem der Ansprüche 3 und 4, dadurch gekennzeichnet, daß das Steuermittel den Schein-Q-Faktor des Resonanzkreises steuert.
6. Stromversorgungsschaltkreis nach Anspruch 5, dadurch gekennzeichnet, daß der Nebenschlußstromkreis Schaltelemente enthält, wodurch im wesentlichen keine Widerstands-Verlustleistung auftritt.
7. Stromversorgungsschaltkreis nach Anspruch 6, dadurch gekennzeichnet, daß der Nebenschlußstromkreis mindestens einen MOS-Transistor (L, Fig. 3; MREG, Fig. 4) enthält.
8. Stromversorgungsschaltkreis nach Anspruch 7, dadurch gekennzeichnet, daß der Nebenschlußstromkreis mehrere Transistoren enthält, die alle die gleiche Polarität besitzen.
9. Stromversorgungsschaltkreis nach irgendeinem vorhergehenden Anspruch, dadurch gekennzeichnet, daß das Steuermittel einen Spannungsvergleicher (X4, Fig. 4) und ein Schalter-Kondensator-Filter (MF1, MF2, MF3, CIN, CLAG, CLEAD1, CLEAD2) enthält.
10. Stromversorgungsschaltkreis nach Anspruch 9, dadurch gekennzeichnet, daß das Schalter-Kondensator-Filter während im wesentlichen der ganzen Periode der Wechselstrom-Signalfom dem Nebenschlußstromkreis ein Treibersignal zuführt.
11. Stromversorgungsschaltkreis nach einem der Ansprüche 9 und 10, dadurch gekennzeichnet, daß der Gleichrichter ein Synchrongleichrichter (X3, M1, M2, M3) ist.
12. Stromversorgungsschaltkreis nach Anspruch 11, dadurch gekennzeichnet, daß das Schalter-Kondensator-Filter und der Synchrongleichrichter durch ein gemeinsames Taktsignal angesteuert werden.
13. Stromversorgungsschaltkreis nach irgendeinem vorhergehenden Anspruch, dadurch gekennzeichnet, daß der Schaltkreis als integrierter Schaltkreis aufgebaut ist.

55 Revendications

1. Circuit d'alimentation en courant destiné à redresser et à réguler une alimentation (S) en courant alter-



natif, comportant un circuit (L) de dérivation et des moyens (A, V) de commande destinés à commander le circuit de dérivation, caractérisé en ce que le circuit (L, figure 3 MREG, figure 4) de dérivation est relié aux bornes de la source alternative du côté alternatif des moyens redresseurs (D, figure 3 ; M1-M3, figure 4).

- 5 2. Circuit d'alimentation en courant selon la revendication 1, caractérisé en ce que les moyens de redressement comportent des moyens (D, figure 3) formant diode et sont couplés à des moyens (C) de stockage de charge.
- 10 3. Circuit d'alimentation en courant selon l'une quelconque des revendications précédentes, caractérisé en ce que la source de courant alternatif comprend un circuit résonnant (LC, figure 3 ; L1-C1, figure 4).
4. Circuit d'alimentation en courant selon l'une quelconque des revendications précédentes, caractérisé en ce que le circuit résonnant est couplé par induction à une source d'alimentation en courant alternatif.
- 15 5. Circuit d'alimentation en courant selon la revendication 3 ou 4, caractérisé en ce que les moyens de commande commandent le facteur Q apparent du circuit résonnant.
- 20 6. Circuit d'alimentation en courant selon la revendication 5, caractérisé en ce que le circuit de dérivation comprend des éléments de commutation, dans lesquels il n'y a pratiquement pas de dissipation de puissance résistive.
7. Circuit d'alimentation en courant selon la revendication 6, caractérisé en ce que le circuit de dérivation comprend au moins un transistor MOS (L, figure 3 ; MREG, figure 4).
- 25 8. Circuit d'alimentation en courant selon la revendication 7, caractérisé en ce que le circuit de dérivation comporte une pluralité de transistors ayant tous la même pluralité.
- 30 9. Circuit d'alimentation en courant selon l'une quelconque des revendications précédentes, caractérisé en ce que les moyens de commande comprennent un comparateur (X4, figure 4) de tension et un filtre à capacité commutée (MF1, MF2, MF3, CIN, CLAG, CLEAD1, CLEAD2).
- 35 10. Circuit d'alimentation en courant suivant la revendication 9, caractérisé en ce que le filtre à capacité commutée fournit un signal d'attaque au circuit de dérivation pendant sensiblement la totalité de la période de la forme d'onde alternative.
- 40 11. Circuit d'alimentation en courant selon la revendication 9 ou 10, caractérisé en ce que les moyens redresseurs sont un redresseur (X3, M1, M2, M3) synchrone.
12. Circuit d'alimentation en courant selon la revendication 11, caractérisé en ce que le filtre à capacité commutée et le redresseur synchrone sont attaqués par un signal d'horloge commun.
- 45 13. Circuit d'alimentation en courant selon l'une quelconque des revendications précédentes, caractérisé en ce que le circuit est intégré.

