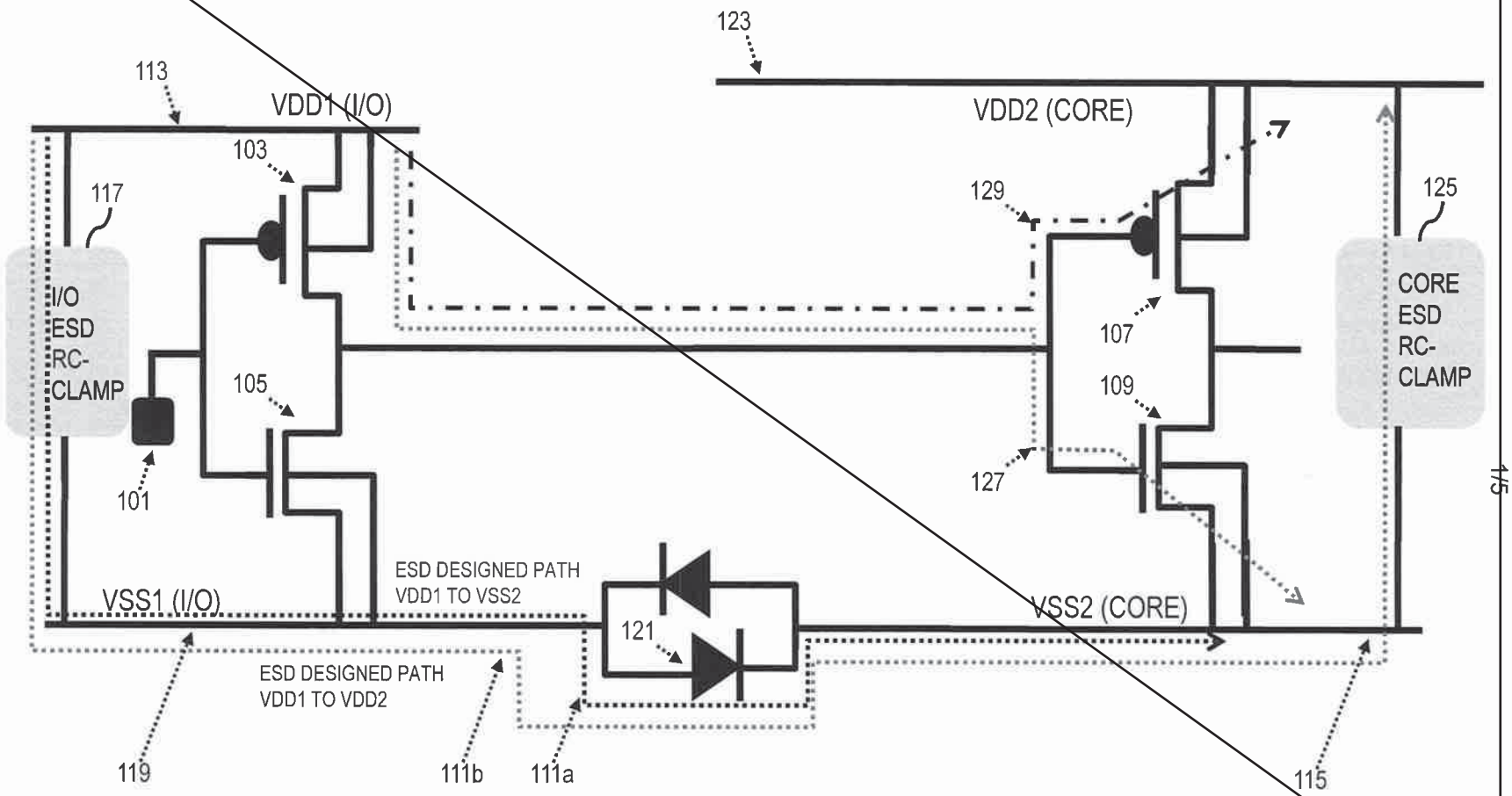
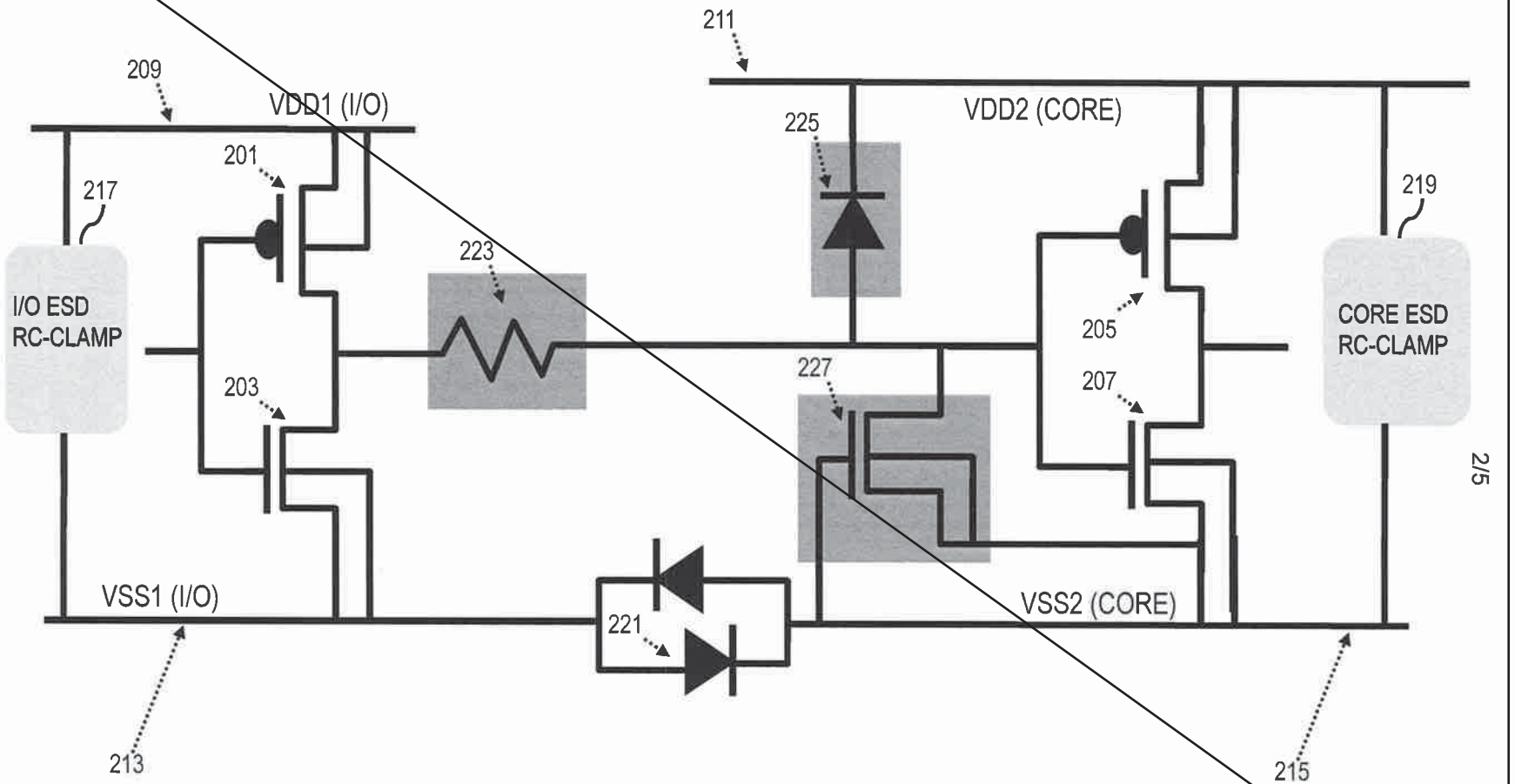
FIG. 1



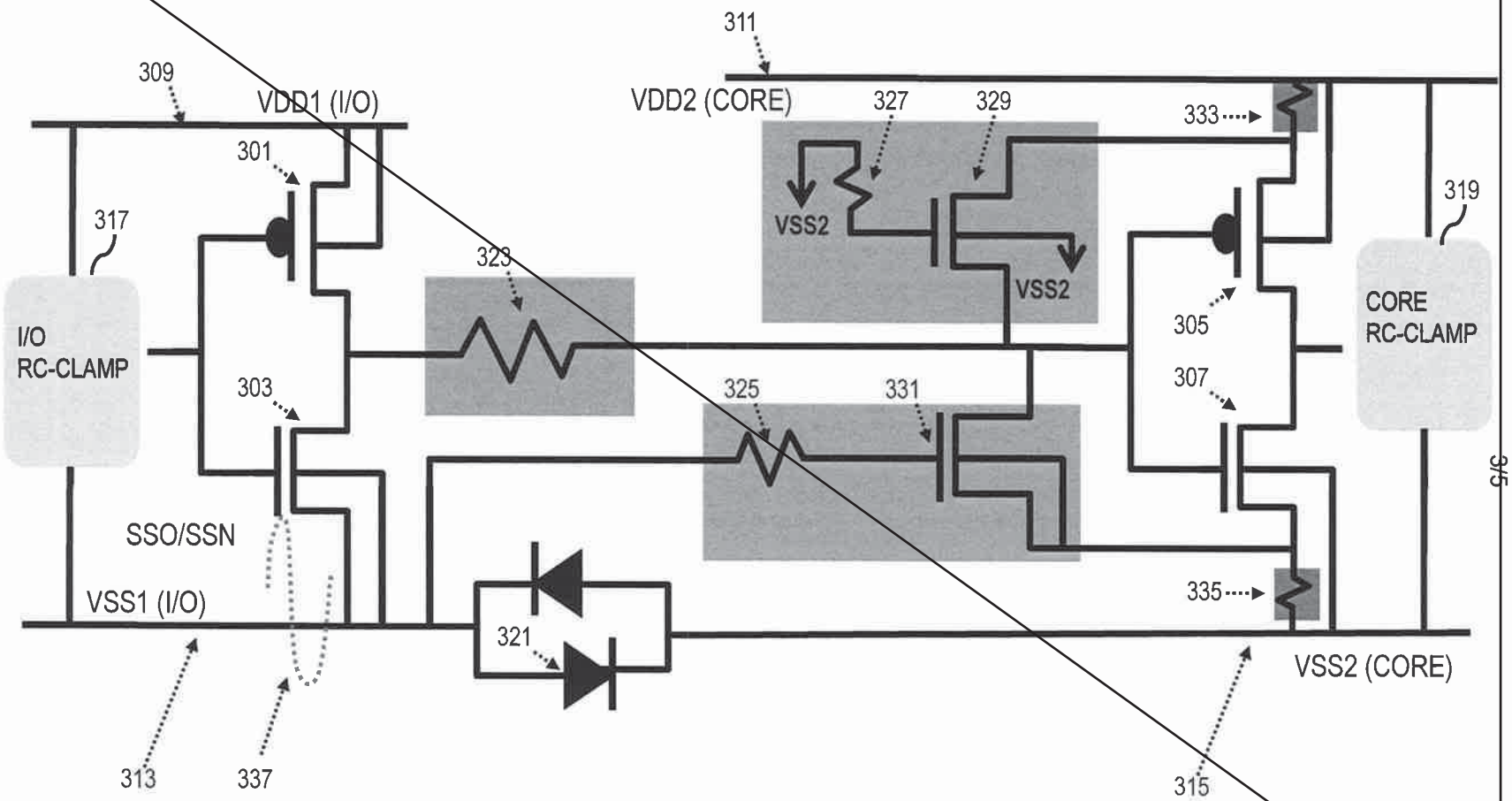
Background Art

FIG. 2



Background Art

FIG. 3



Background Art

FIG. 4A

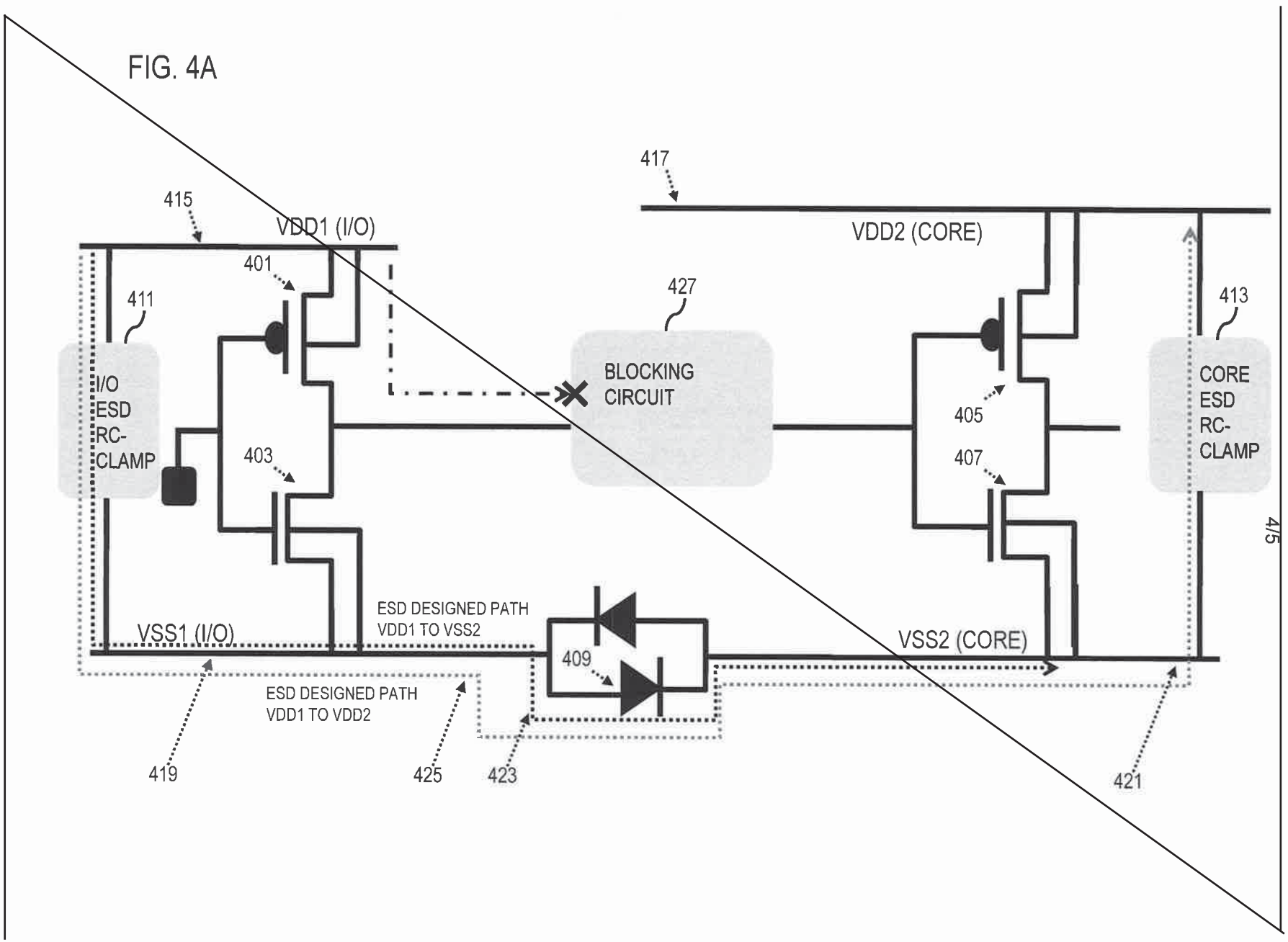
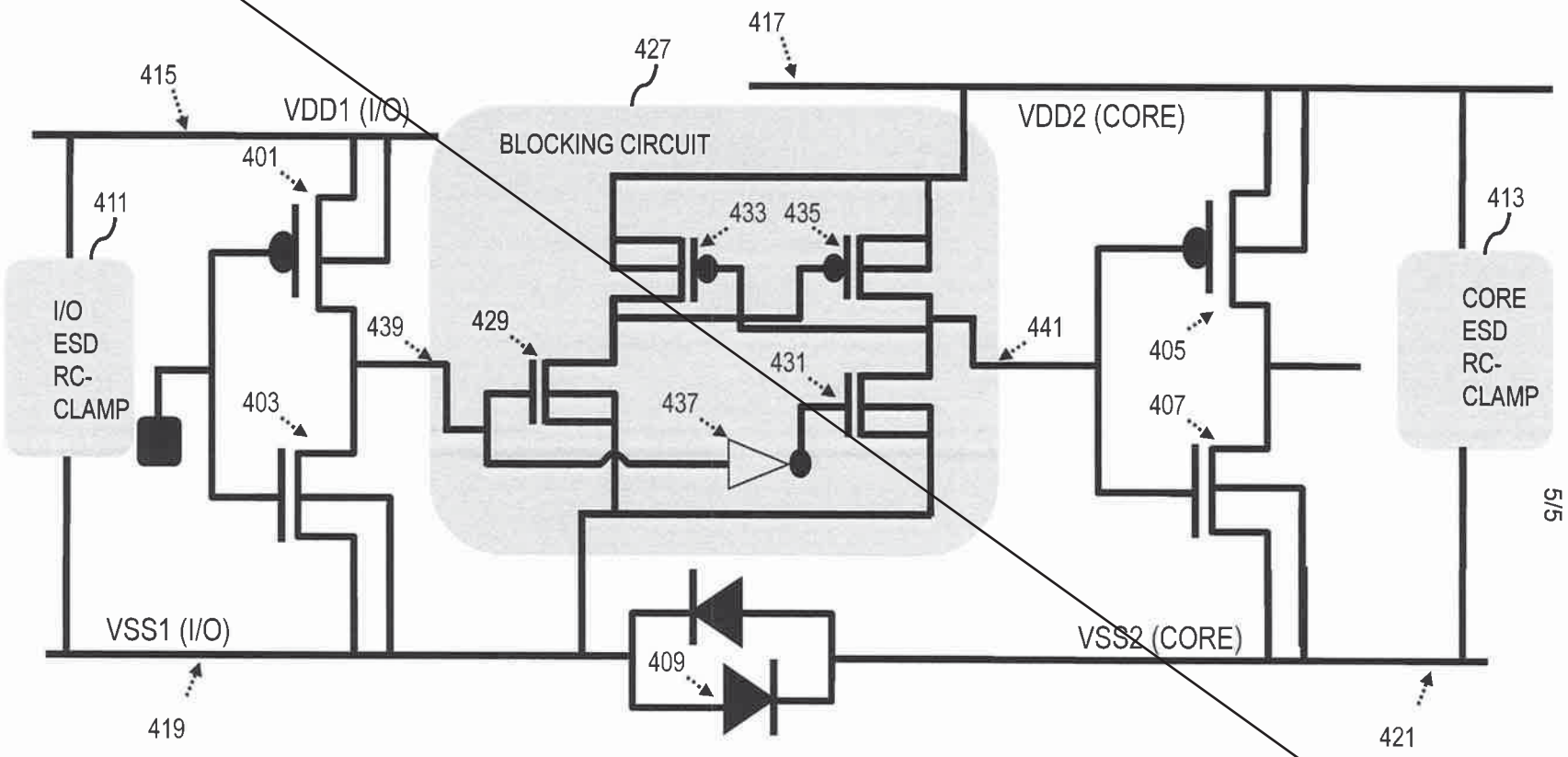

415
VDD1 (I/O)
417
VDD2 (CORE)
401
411
427
413
I/O
ESD
RC-
CLAMP
BLOCKING
CIRCUIT
CORE
ESD
RC-
CLAMP
405
403
407
ESD DESIGNED PATH
VDD1 TO VSS2
VSS1 (I/O)
VSS2 (CORE)
409
ESD DESIGNED PATH
VDD1 TO VDD2
419
425
423
421

FIG. 4B


415
VDD1 (I/O)
427
BLOCKING CIRCUIT
417
VDD2 (CORE)
401
411
433
435
413
I/O
ESD
RC-
CLAMP
439
429
441
405
CORE
ESD
RC-
CLAMP
431
403
437
407
VSS1 (I/O)
409
VSS2 (CORE)
419
421

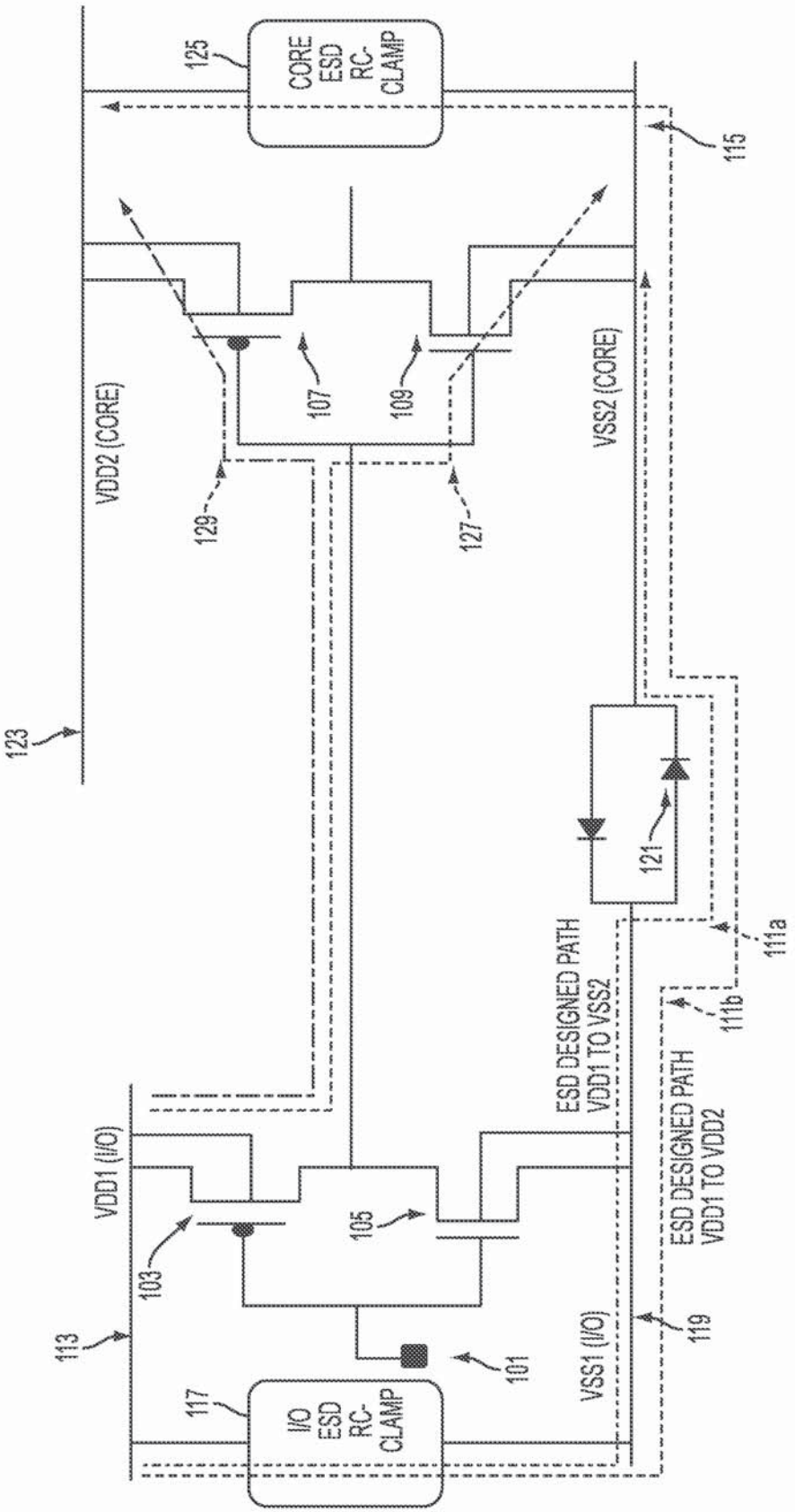


FIG. 1
BACKGROUND ART

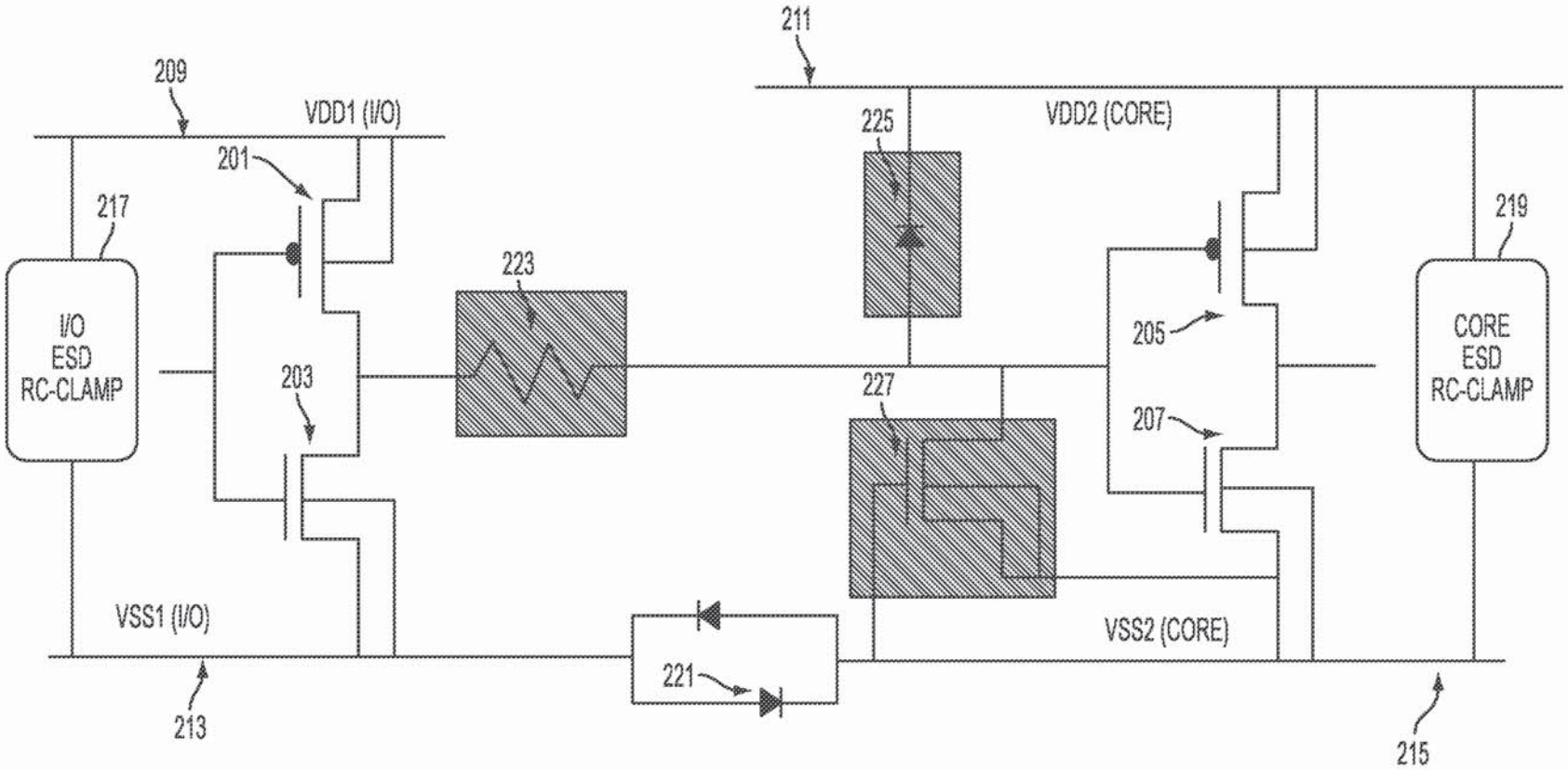


FIG. 2
BACKGROUND ART

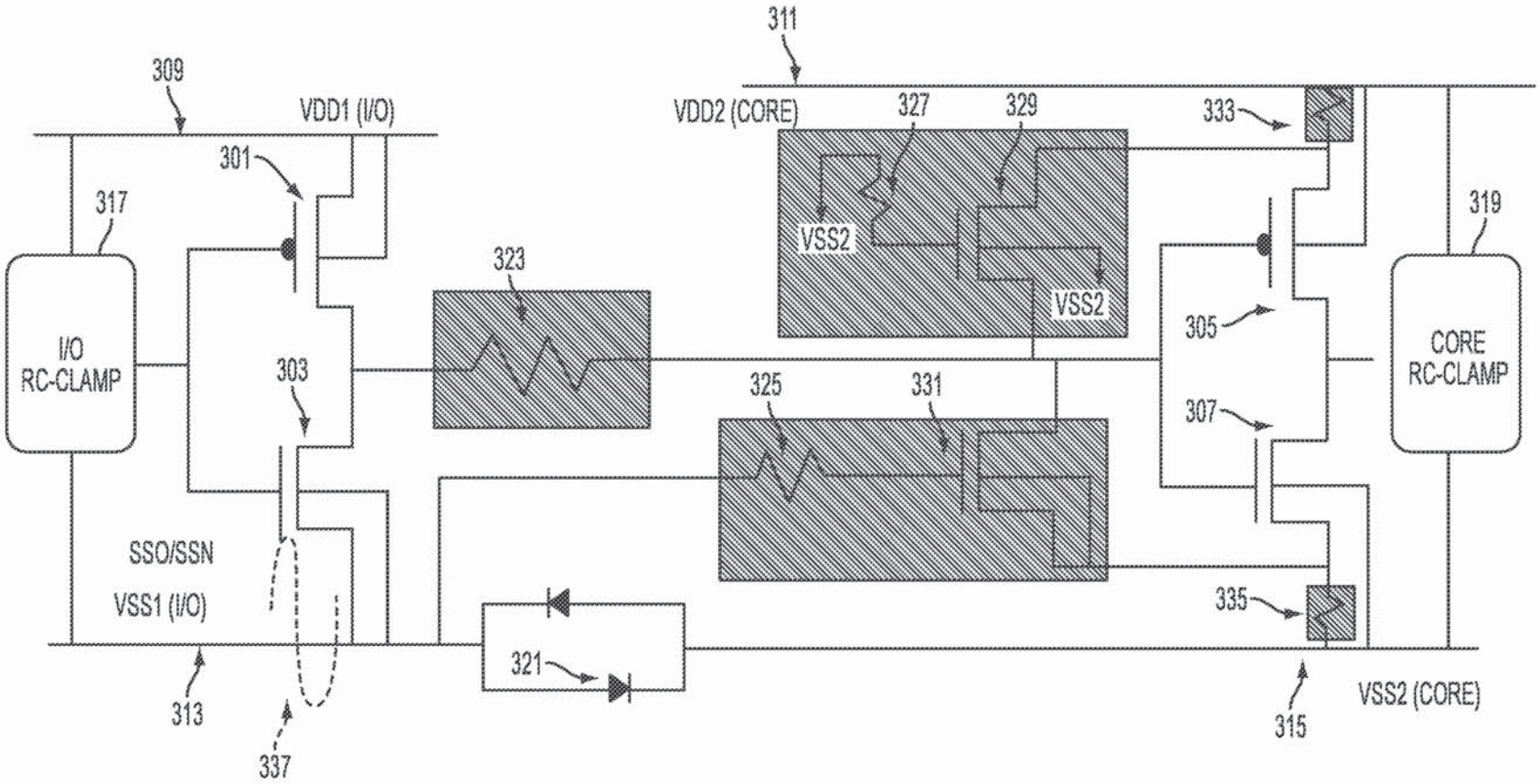


FIG. 3
BACKGROUND ART

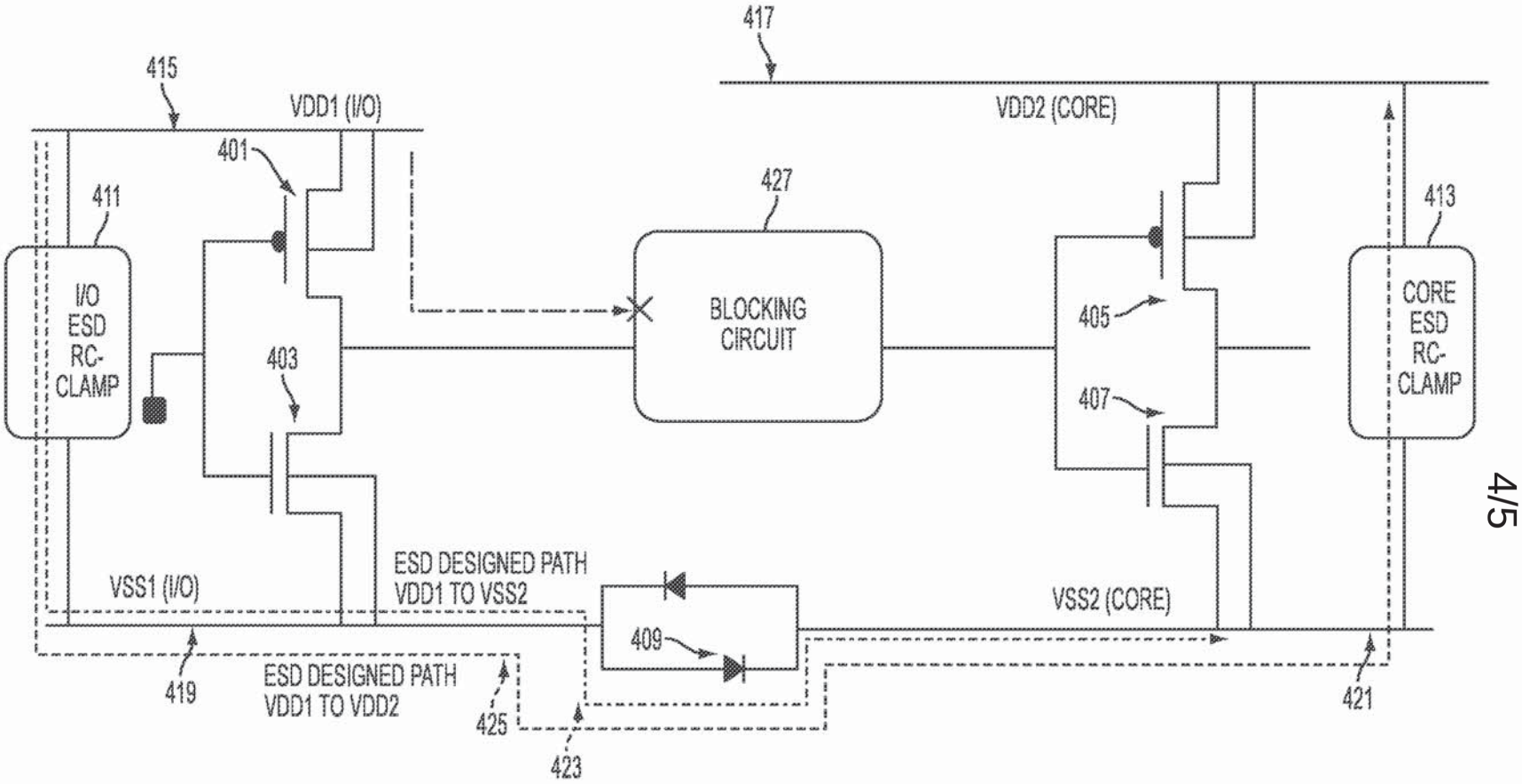

417
415
VDD1 (I/O)
VDD2 (CORE)
401
427
411
413
I/O
ESD
RC-
CLAMP
BLOCKING
CIRCUIT
405
403
407
CORE
ESD
RC-
CLAMP
ESD DESIGNED PATH
VDD1 TO VSS2
VSS1 (I/O)
VSS2 (CORE)
409
419
ESD DESIGNED PATH
VDD1 TO VDD2
425
421
423

FIG. 4A

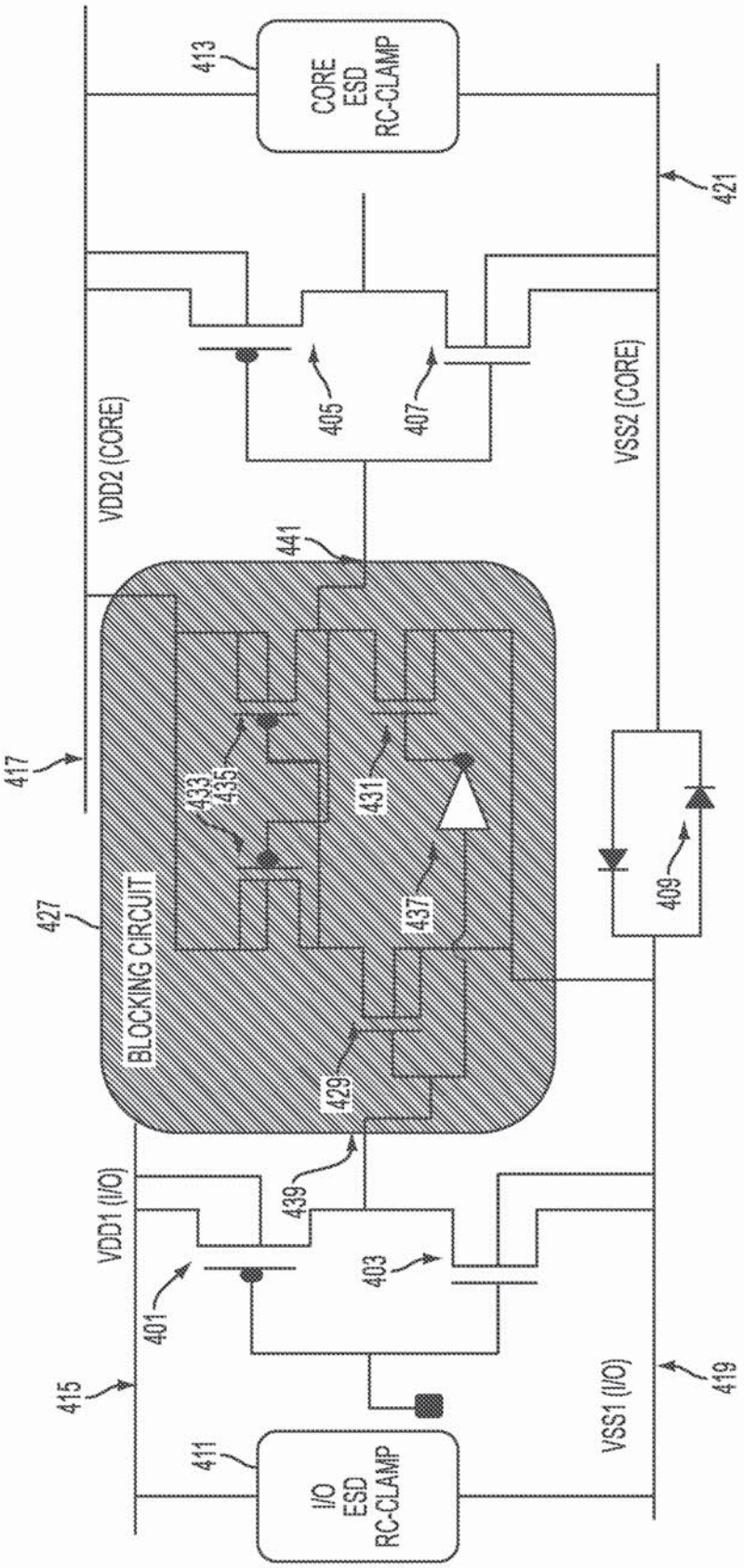

CORE ESD RC-CLAMP
413
421
VDD2 (CORE)
VSS2 (CORE)
405
407
441
417
433
435
431
427
BLOCKING CIRCUIT
437
429
409
439
VDD1 (I/O)
403
401
415
411
I/O ESD RC-CLAMP
VSS1 (I/O)
419

FIG. 4B