A PARTIALLY RECESSED SHALLOW TRENCH ISOLATION METHOD FOR FABRICATING BORDERLESS CONTACTS

ABSTRACT

An improved and new process for fabricating MOSFET's in shallow trench isolation (STI), with sub-quarter micron ground rules, includes a passivating trench liner of silicon nitride. The silicon nitride passivating liner is utilized in the formation of borderless or "unframed" electrical contacts, without reducing the poly to poly spacing. Borderless contacts are formed, wherein contact openings are etched in an interlevel dielectric (ILD) layer over both an active region (P-N junction) and an inactive trench isolation region. During the contact hole opening, a selective etch process is utilized which etches the ILD layer, while the protecting passivating silicon nitride liner remains intact protecting the P-N junction at the edge of trench region. Subsequent processing of conductive tungsten metal plugs are prevented from shorting by the passivating trench liner. This method of forming borderless contacts with a passivating trench liner in a partially recessed trench isolation scheme improves device reliability since it prevents electrically short circuiting of the P-N junction and lowers the overall diode leakage. In addition, the use of this invention's semi-recessed STI process scheme helps to reduce the aspect ratio of the trench, thereby aiding the filling of the trench. Therefore, with the process described herein, STI oxide seam formation is eliminated.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)