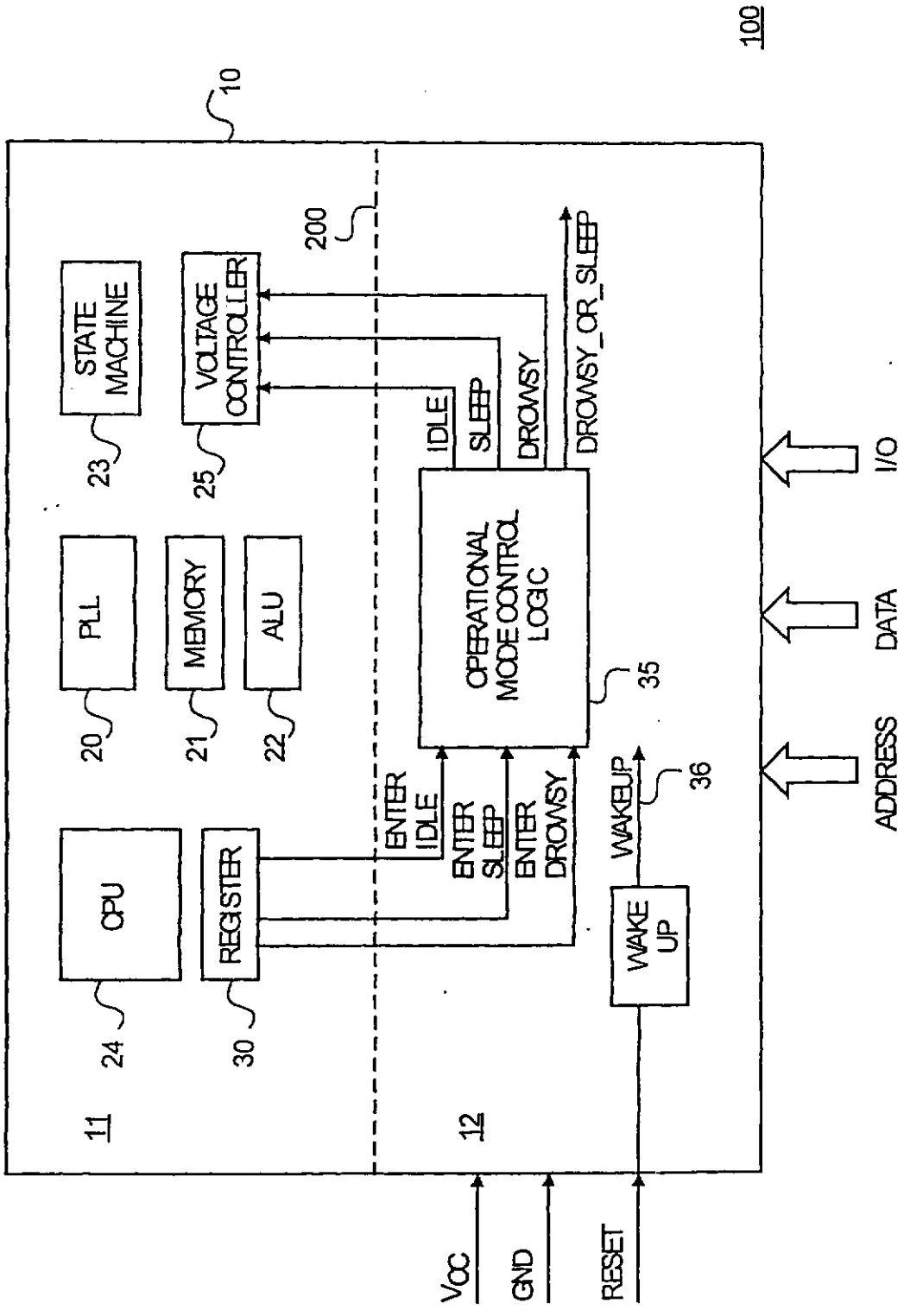

100
10
200
STATE MACHINE
23
VOLTAGE CONTROLLER
25
IDLE
SLEEP
DROWSY
DROWSY_OR_SLEEP
PLL
20
MEMORY
21
ALU
22
OPERATIONAL MODE CONTROL LOGIC
35
I/O
DATA
ADDRESS
CPU
24
REGISTER
30
ENTER IDLE
ENTER SLEEP
ENTER DROWSY
WAKEUP
36
WAKE UP
11
12
VCC
GND
RESET

FIG. 1

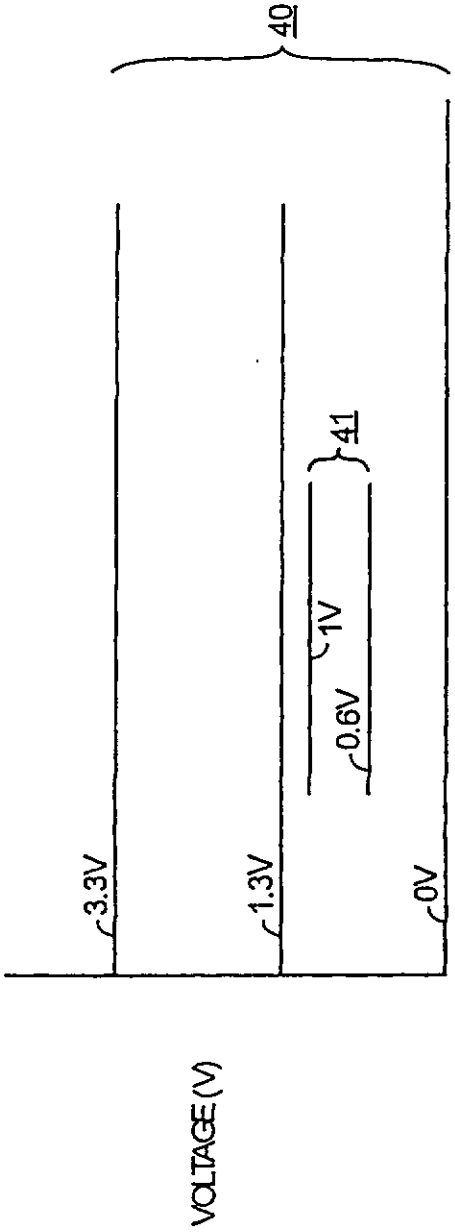


FIG 2

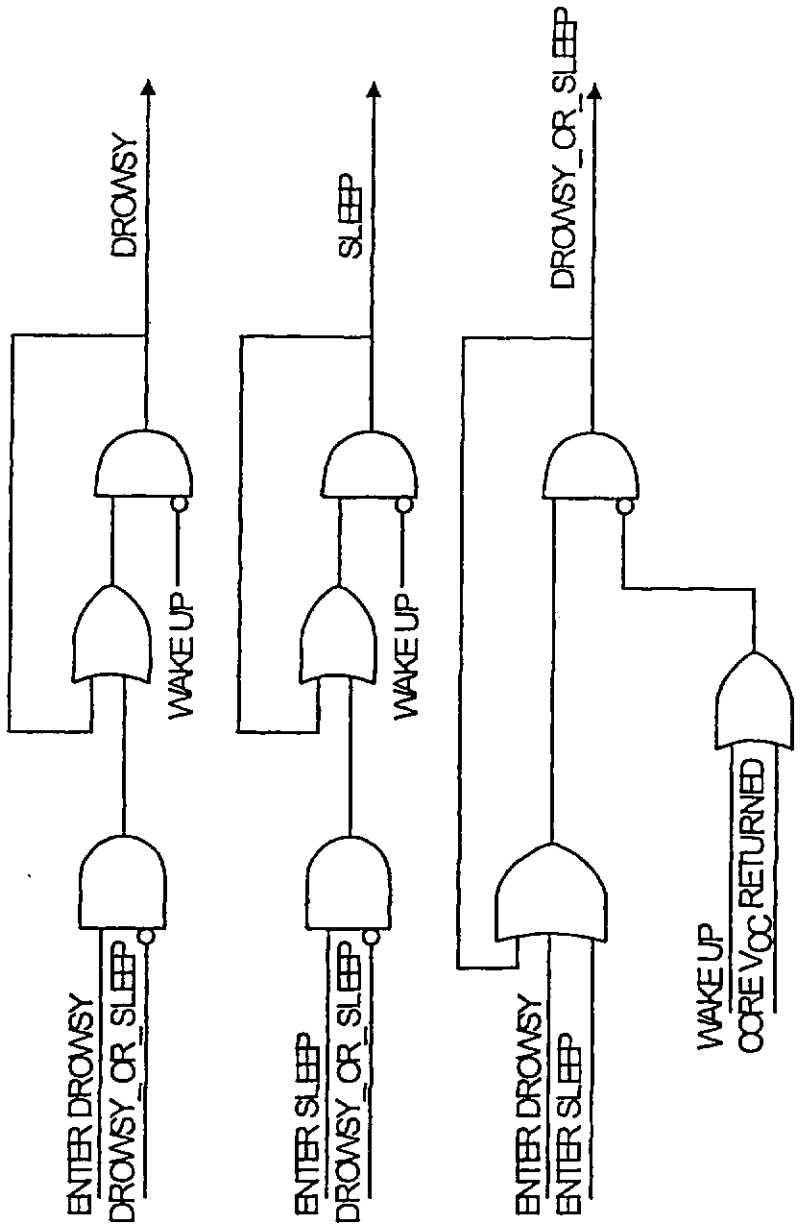

DROWSY
WAKE UP
ENTER DROWSY
DROWSY_OR_SLEEP
SLEEP
WAKE UP
ENTER SLEEP
DROWSY_OR_SLEEP
DROWSY_OR_SLEEP
ENTER DROWSY
ENTER SLEEP
WAKE UP
CORE V_{DC} RETURNED

FIG. 3

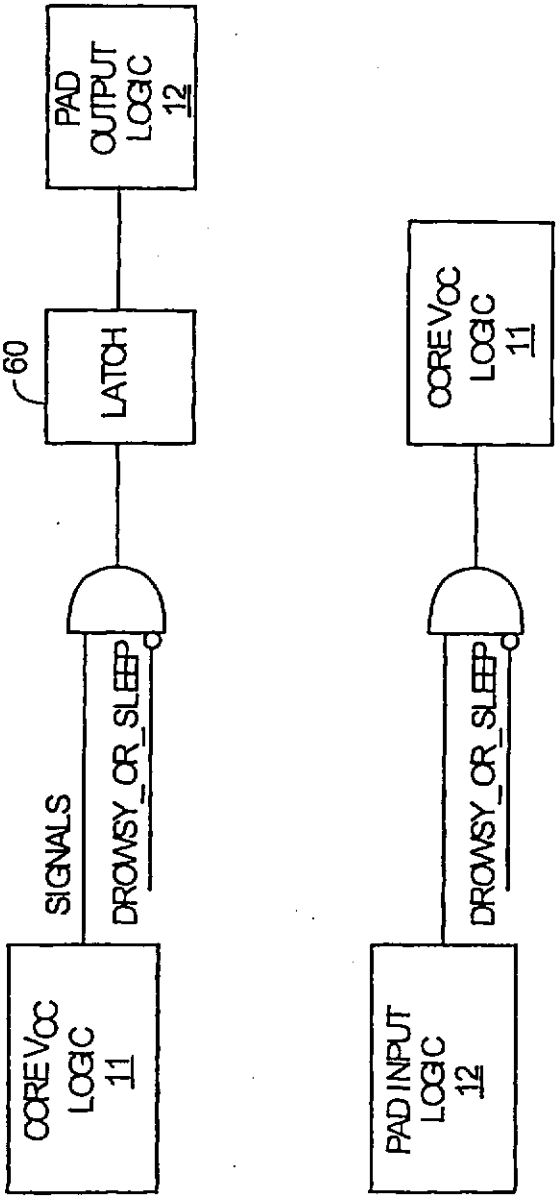

PAD OUTPUT LOGIC 12
60
LATCH
CORE VCC LOGIC 11
SIGNALS
DROWSY_OR_SLEEP
CORE VCC LOGIC 11
PAD INPUT LOGIC 12
DROWSY_OR_SLEEP

FIG 4