A DISPLAY DRIVER

Field of the Invention

This invention relates to storing display data in a display driver, and more particularly to storing the display data using an addressing arrangement which is different from that used for displaying the display data.

Background of the Invention

As is known, a display driver receives pixel display data that represent an image and commands, and provides pixel addressing data bits to a display, such as a liquid crystal display (LCD), which has an array of picture elements or pixels arranged in rows and columns. The commands control the display driver to switch the pixels to display the image. When the pixel display data is received, it is stored in a memory in the display driver.

In a conventional display driver, the memory has addressable storage locations which are addressed by row and column addresses. A row and column address addresses both the storage location of the pixel display data in the memory and a corresponding pixel on the display. To switch the pixel ON or OFF the row and column address of the pixel or pixel addressing data bits of the pixel are provided to the LCD.

For example, when the LCD has pixels arranged in a 33 row by 120 column array, the memory in the display driver has storage locations with row and column addresses that correspond to the 33 rows and 120 columns of pixels on the LCD. Consequently, display drivers tend to be dedicated devices which can only be used with LCDs having a predetermined arrangement of pixels that correspond with the addressing arrangement of storage locations in the memory of the display driver.

Further, storing the display data in the memory of a display driver in this way, restricts the degree to which the displayed image on the LCD may be manipulated.

Brief Summary of the Invention

The present invention therefore seeks to provide a display driver that can be used with a variety of displays having different pixel arrangements, and which enhances the degree of manipulation of the displayed image.

Accordingly, in one aspect the invention provides a display driver comprising: a memory comprising: a pixel display data input; an address input; and a pixel display data output; a processor comprising: a memory address output coupled to the address input of the memory; a pixel display data input coupled to the pixel display data output of the memory; a display address output; and a pixel addressing data bits output; and an addressable register comprising: an display address input coupled to the display address output of the processor; a pixel addressing data bits input coupled to the pixel addressing data bits output of the processor; and a pixel address data output.

In another aspect the present invention provides a method for storing pixel display data in a display driver for a display, the method comprising the steps of: receiving a display command and corresponding pixel display data; storing the pixel display data in a memory in accordance with both the display command and a first predetermined addressing arrangement; selectively retrieving the pixel display data from the memory in accordance with a second predetermined addressing arrangement; processing the retrieved pixel display data for display in accordance with a predetermined display process to produce pixel addressing data bits; storing the pixel addressing data bits in an addressable register in accordance with a third predetermined addressing arrangement, wherein the pixel addressing data bits are arranged in the addressable register to

form at least one pixel address; and providing the at least one pixel address at a pixel address data output for a display.

Brief Description of the Drawings

An embodiment of the invention will now be more fully described, by way of example, with reference to the drawings of which:

FIG. 1 illustrates a block diagram of a display driver in accordance with the present invention; and

FIG. 2 illustrates a schematic diagram of the operation of the display driver in FIG. 1.

Detailed Description of the Drawings

In FIG. 1 a display driver circuit 3 has a command decoder 6 coupled to received commands from a host processor (not shown), such as a microprocessor or a display processor. The command decoder 6 is a serial to parallel converter with a serial port and a parallel port. The serial port supports a serial interface (SPI) to communicate commands and configuration information from the host processor, and to communicate status information to the host processor. The parallel port of the command decoder 6 is coupled to an addressable register memory 8 to communicate commands, configuration information and status information therebetween.

The addressable register memory 8 is coupled to communicate with a digital signal processor (DSP) 12 via an input bus 11, and via a row and column select bus 13 with a voltage generator 28 and a row and column control and voltage select logic circuit 17. The addressable register memory 8 has several internal registers, including a command register (not shown) where commands are stored. The command register is bit readable and this allows the DSP 12 to selectively retrieve commands in the command register. In addition, the addressable register memory 8 also has an output which provides an update signal to the DSP 12 whenever contents in the addressable register memory 8 are changed, for example, when a command is received from the host processor. The DSP 12 responds to the update signal by reading the contents of the addressable

register memory 8 and reacting accordingly. For example, if the contents includes a command, then the DSP 12 prepares to execute the command.

The voltage generator 28 generates liquid crystal display (LCD) voltages for an LCD (not shown) to which the display driver circuit 3 is coupled. The voltage generator 28 is provided with a single voltage supply input and generates necessary bias voltages (VL1-VLN). The voltage generator 28 is software controllable by configuration information provided via the row and column select bus 13 from the addressable register memory 8.

The DSP 12 retrieves the commands in the command register via the input bus 11. Also, via the input bus 11, the DSP 12 provides addresses to a pixel addressable memory 22. Pixel display data that represents an image for display on the LCD are received on the input bus 11 and stored in the pixel addressable memory 22 at storage locations indicated by the addresses provided by the DSP 12. The DSP 12 generates the addresses for storing the pixel display data using information provided during an initial configuration process which will be described later. Essentially, from the configuration information the DSP 12 determines the format in which the pixel display data will be provided via the input bus 11 and programs itself to provide addresses to store the pixel display data in sequential storage locations of the pixel addressable memory 22.

The pixel addressable memory 22 is a I x J x N bits memory, where I and J define the array of storage locations for each of a corresponding array of pixels on the LCD. N determines the number of data bits that are stored for each of the pixel display data. Where the number of rows and columns on a display are X and Y, then the relationship between the number of storage locations required in the pixel addressable memory 22 for the LCD is given below.

$$I \times J > (\text{int}((X+Y)/2))^2, \text{ when } N = 1$$

The DSP 12 also provides a clock configuration signal to a timing generator 23, and receives a clock signal from the timing generator 23. The timing generator 23 also provides a liquid crystal control signal (M) to a

voltage select circuit 18, a serial clock signal (SCLK) to the row and column control and voltage select logic circuit 17, and a line pulse signal (LP) to a data latch 16. The timing generator 23 is an on chip low power resistor-capacitor (RC) oscillator. The oscillator frequency can be selected within the range of 15 - 5000 kilohertz (kHz) by an external resistor (not shown). The timing generator 23 can also be enabled by a software command. Optionally, an external clock signal can be provided to the driver circuit 3.

The DSP 12 is coupled to an addressable display register 15 via an output bus 14. The DSP 12 retrieves the pixel display data from the pixel addressable memory 22 using the same addressing arrangement with which the pixel display data was stored. The DSP 12 then processes the pixel display data to produce pixel addressing data bits X, Y and P which are selectively stored, via the output bus 14, in the addressable display register 15. The X data bits address the columns of the pixels on the LCD, the Y data bits address the rows of the pixels on the LCD, and the P data bits address annunciators (not shown) on the LCD. The X data bits determine whether a corresponding pixel on the display is switched ON or OFF, thus by addressing a pixel with the corresponding X data bits and Y data bits associated with that pixel, that pixel is switched ON.

When the DSP 12 has completed storing the X, Y and P pixel addressing data bits associated with a pixel display data bit stored in the pixel addressable memory 22, the X,Y and P pixel addressing data bits in the addressable display register 15 are provided as pixel address data from a pixel address data output to a data latch 16.

The pixel address data output of the addressable display register 15 is a parallel data output that provides the X, Y and P pixel addressing data bits to the data latch 16 that latches the X, Y and P pixel addressing data bits in accordance with the line pulse signal (LP). Latching the X, Y and P pixel addressing data bits leaves the addressable display register 15 available for the DSP 12 to store subsequent X,Y and P pixel addressing data bits in the addressable display register 15.

The data latch 16 provides the latched pixel addressing data bits X, Y and P to the row and column control and voltage select logic circuit 17. During an initial configuration process, which will be described later, row and column configuration data in a row and column configuration register (not shown) in the addressable register memory 8 is provided to the row and column control and voltage select logic circuit 17 via the row and column select bus 13. The row and column configuration data configures the row and column control and voltage select logic circuit 17 to provide output that are suitable for driving a particular LCD. Among other parameters, the number of X, Y and P pixel addressing data bits are configured to match the X, Y and P pixel addressing data bits input of the particular LCD that is to be coupled to and driven by the driver circuit 3. The DSP 12 also uses the row and column configuration data to control the Y pixel addressing data bits in the addressable display register 15. In this way the DSP 12 controls the display of rows of pixels on the LCD by rotating a fixed bit pattern according to the line pulse (LP) signal from the timing generator 23.

The voltage select circuit 18 includes a bank of multiplexors, and the configuration process switches the multiplexors so that outputs provided for each of the X or Y or P pixel addressing data bits are suitable in polarity and voltage level for the particular LCD. This is necessary as the X, Y and P pixel addressing data bits input for different LCDs have different polarity and voltage level requirements.

The voltage select circuit 18 generates a voltage pattern for each of the X, Y and P pixel addressing data bits by selecting from among the range of voltage levels (VL1-VLN) in accordance with the timing information of the serial clock (SCLK). The voltage generator 28 is configured by configuration information from the addressable register memory 8 via the row and column select bus 13 to provide the range of voltage levels (VL1-VLN) to the voltage select circuit 18.

The voltage patterns for each of the X, Y and P bits are provided by the voltage select circuit 18 to a driver circuit 19 that amplifies the voltage

patterns to levels that are suitable for driving the particular LCD. It is anticipated that the amplification may also be made programmable or adjustable to suit different input level requirements of different LCDs.

The host processor is coupled to the command decoder 6 and the input bus 11 of the DSP 12. From the host processor pixel display data is provided to the DSP 12 via the input bus 11 and commands are provided to the DSP 12 via the command decoder 6 and the addressable register memory 8. When a command is stored in the command register in the addressable register memory 8, the addressable register memory 8 provides the update signal to the DSP 12. In response, the DSP 12 retrieves the command stored in the command register of the addressable register memory 8 via the input bus 11, and prepares to execute the commands accordingly.

During the configuration process, the host processor sends commands to the driver circuit 3 to configure it for use with the particular LCD. The commands include the number of pixels on the LCD, the number of pixels in each row and in each column of the LCD, the liquid crystal control signal (M) setting required for the LCD, and various other parameters of the particular LCD. Also, as described earlier, configuration information is stored in the command register in the addressable register memory 8 to configure the row and column control and voltage select logic circuit 17 and the voltage generator 28.

The DSP 12 also uses the configuration information to determine the arrangement in which the pixel display data is to be stored and retrieved in the pixel addressable memory 22. When pixel display data is received on the input bus 11 by the DSP 12, the DSP 12 stores the received pixel display data in the pixel addressable memory 22 in accordance with the predetermined arrangement. Generally, the pixel display data is stored in sequentially addressed storage locations of the pixel addressable memory 22. In addition, the DSP 12 uses the configuration information to determine an addressing arrangement with which the pixel display data is to be retrieved from the pixel addressable memory 22. The configuration

information also determines the way in which the retrieved pixel display data is to be processed for display, and also determines yet another addressing arrangement with which the X, Y and P pixel addressing data bits are to be stored in the addressable display register 15. Generally, several store operations are required to store the X, Y and P pixel addressing data bits in the addressable display register 15. The X, Y and P pixel addressing data bits are then provided as pixel address data from the pixel address data output by the addressable display register 15 to the data latch 16. The latched pixel addressing data bits are provided by the data latch 16 to the row and column control and voltage select logic circuit 17 which provides X, Y and P pixel addressing data bits that are suitable for addressing pixels on the LCD. The voltage select circuit 18 receives the X, Y and P pixel addressing data bits and provides switching voltage patterns for the X, Y and P pixel addressing data bits. The X, Y and P switching voltage patterns are amplified by the amplifier 19 and provided to the LCD where the amplified X, Y and P switching voltage patterns selectively switch the pixels on the LCD to display the image represented by the pixel display data stored in the pixel addressable memory 22.

With reference to FIGS. 1 and 2, an LCD 40 has X columns and Y rows of pixels or X by Y pixels which are addressable using the respective X,Y pixel addressing data bits. The pixel addressable memory 22 has sequentially addressable storage locations that store the pixel display data for each of the corresponding pixels. The pixel display data indicates which of the pixels are switched ON and which are switched OFF. When the pixel display data is a bit representing a logic 1 the corresponding pixel is switched ON, and when the bit represents a logic 0, the corresponding pixel is switched OFF. In this way an image is displayed on the LCD.

When the display driver circuit 3 is configured to drive the display 40, the DSP 12 is configured or programmed to receive the pixel display data on the input bus 11 in a predetermined sequential order. The sequence begins with pixel display data for pixel (0,0) 41, proceeds with pixel display data for the other pixels along row 0 i.e. for pixels (1,0) and (2,0) 42 etc.

until pixel display data for the last pixel on row 0 i.e. (X,0) 43 is reached. The sequence of pixel display data continues with the receipt of pixel display data for the next row i.e. row 1 for pixel (0,1) 44 until pixel (x,1) 45. This input of pixel display data continues until the pixel display data for the last row of pixels (0,y) 46 to (X,Y) 47 is received.

As pixel display data is received, the DSP 12 stores them in sequentially addressable storage locations 50 in the pixel addressable memory 22. The first storage location having address 0 stores the pixel display data for pixel (0,0) 41 and the following sequentially addressable storage locations having addresses 1 to X stores the pixel display data for pixels in row 0 from (1,0) 42 to (x,0) 43. The subsequent sequentially addressable storage locations having addresses X +1 to X +X stores the pixel display data for the next row of pixels (0,1) 44 to (X,1) 45.

To display the image represented by the stored pixel display data, the DSP 12 retrieves the stored pixel display data from the pixel addressable memory 22 using the same sequential addressing arrangement that was used for storing the pixel display data. Depending on how the stored pixel display data is to be displayed, a different addressing arrangement can be used to retrieve the stored pixel display data. The DSP 12 then processes the retrieved pixel display data to produce the pixel addressing data bits comprising the X,Y and P data bits, and the DSP 12 stores the X,Y and P pixel addressing data bits in the addressable display register 15 in accordance with yet another addressing arrangement.

When the pixel addressable memory 22 has a matrix of storage locations which is I x J and the total number of pixels on the LCD 40 i.e. X x Y is less than I x J, then the storage locations having addresses beyond the address X x Y i.e. the next storage location 52 until the storage location having address I x J (54), is left blank.

Hence, the DSP 12, in accordance with the present invention, controls the storage and retrieval of pixel display data to and from the pixel addressable memory 22 in the display driver circuit 3, to advantageously

store the pixel display data bits in a manner which is independent of the arrangement of the pixels on the LCD 40.

There may be instances where the pixel display data provided by the host processor (not shown) to the display driver circuit 3 is intended for a smaller LCD with less pixels than the LCD that is coupled to the display driver circuit 3. In such a situation, the number of pixels in a row represented by the retrieved pixel display data will be less than the number of pixels in a row on the display, and a narrower image is displayed on the LCD. An interpolation process may be used to add pixels, between the pixels provided by the pixel display data, with dummy data bits to increase the number of pixels per row provided by the pixel display data to become equal to the number of pixels in a row of the LCD.

Alternatively there may be instances when the pixel display data provided by the host processor (not shown) to the display driver circuit 3 is intended for a larger LCD with more pixels than the LCD that is coupled to the display driver circuit 3. The number of pixels in a row represented by the retrieved display data bits will then be greater than the number of pixels in a row on the LCD. Consequently, only a portion of the image represented by the stored pixel display data can be displayed on the LCD. Provisions can be made to allow a viewer to manoeuvre the displayed portion of the image to view the entire image represented by the store pixel display data. Alternatively, a process may be used to drop the stored pixel display data to reduce the number of pixels in a row provided by the pixel display data to equal the number of pixels in a row on the LCD.

The pixel addressable memory 22 stores a complete frame of pixel display data. The DSP 12 can selectively retrieve the pixel display data, and selectively re-store the retrieved pixel display data in the addressable display register 15. The contents of the addressable display register 15 will then be copied to the data latch 16 for further processing according to the line pulse signal (LP) triggering. Consequently, this addressing arrangement allows the DSP 12 to manipulate the way the image

represented by the pixel display data is displayed by the pixels on the LCD 40.

For example, a displayed image can be rotated by 90,180 and 270 degrees using modulo addressing, and even rotated by any particular degree using modified modulo addressing. The display driver circuit 3 can also support a blinking cursor and even multiple blinking cursors. In addition, a 2-line addressing method, such as the 2D Walsh Matrix Operation for LCD panels, which reduces the driving voltage by half, can also be employed.

The row and column control and voltage select logic circuit 17 advantageously allows the row and column outputs of the display driver circuit 3 to be changed. Hence, the display driver circuit 3 can be used with LCDs having a variety of pixel arrangements. For example, when the appropriate parts of the display driver circuit 3 supports 153 + P data bits and storage locations, the display driver circuit 3 can be used with LCDs having a variety of pixel arrangements including 8X145,76X76,145X8 pixels, or 76X76 pixels with split panel. Indeed, any LCD where X + Y is equal to 153 pixels.

Further, the flexible addressing capability of the DSP 12 enables different functions such as vertical scrolling, cursor control and grey scale generation to be performed by the display driver circuit 3.

The present invention advantageously allows a display driver circuit to be used for displays having a variety of different pixel arrangements. This is accomplished with a DSP that controls the arrangement of display data bits that are stored to, and retrieved from, a pixel addressable memory.

The present invention therefore provides a display driver circuit that can be used with a variety of displays having different pixel arrangements, and provides enhanced display features for manipulating the displayed image.

Claims

1. A display driver comprising:

a memory comprising:

a pixel display data input;

an address input; and

a pixel display data output;

a processor comprising:

a memory address output coupled to the address input of the memory;

a pixel display data input coupled to the pixel display data output of the memory;

a display address output; and

a pixel addressing data bits output; and

an addressable register comprising:

a display address input coupled to the display address output of the processor;

a pixel addressing data bits input coupled to the pixel addressing data bits output of the processor; and

a pixel address data output.

2. A display driver according to claim 1 wherein:

the memory comprises a memory means for receiving pixel display data and at least one storage address, and for storing the pixel display data at the at least one storage address;

the processor comprises a processor means for providing the at least one storage address, for retrieving the pixel display data from the memory means, for processing the retrieved pixel display data to produce a plurality of pixel addressing data bits, and for selectively providing at least one of a plurality of display addresses and at least some of the plurality of pixel addressing data bits; and

the addressable register comprises an addressable register means for receiving the at least one of the plurality of display addresses and the at

least some of the plurality of pixel addressing data bits, for storing the at least some of the plurality of pixel addressing data bits at the at least one of the plurality of display addresses, and for providing the plurality of pixel addressing data bits stored at the plurality of display addresses to the pixel address data output.

3. A display driver comprising:

a memory means for receiving pixel display data and at least one storage address, and for storing the pixel display data at the at least one storage address;

a processor means coupled to the memory means for providing the at least one storage address, for retrieving the pixel display data from the memory means, for processing the retrieved pixel display data to produce a plurality of pixel addressing data bits, and for selectively providing at least one of a plurality of display addresses and at least some of the plurality of pixel addressing data bits; and

an addressable register means coupled to the processor means for receiving the at least one of the plurality of display addresses and the at least some of the plurality of pixel addressing data bits, for storing the at least some of the plurality of pixel addressing data bits at the at least one of the plurality of display addresses, and for providing the plurality of pixel addressing data bits to a pixel address data output.

4. A display driver in accordance with claim 3 further comprising an input bus means coupled to the memory means and the processor means for communicating the pixel display data and the at least one storage address thereon.

5. A display driver in accordance with claim 3 further comprising an output bus coupled to the processor means and the addressable register means for communicating the plurality of pixel addressing data bits and the plurality of display addresses thereon.



6. A display driver in accordance with claim 3 further comprising a data latch means coupled to the pixel address data output of the addressable register means for receiving and storing the plurality of pixel addressing data bits, and having an output for providing the plurality of pixel addressing data bits.

7. A display driver in accordance with claim 6 further comprising a control and voltage select logic circuit means coupled to the output of the data latch means to receive the plurality of pixel addressing data bits and having an input for receiving configuration information, and the control and voltage select logic circuit means having an output for providing at least row addressing data bits and column addressing data bits for a display means.

8. A display driver in accordance with claim 7 further comprising a voltage select circuit means coupled to the output of the control and voltage select logic circuit means to receive the at least row addressing data bits and column addressing data bits, the voltage select circuit means having a plurality of inputs for receiving a corresponding plurality of input voltage levels and having an output for providing a plurality of switching voltage patterns for selectively switching the pixels on the display means.

9. A display driver in accordance with claim 8 further comprising an amplifier means coupled to the output of the voltage select circuit means to receive the of switching voltage patterns and having an output for providing amplified switching voltage patterns for the display means.

10. A display driver in accordance with claim 9 further comprising a timing generator means coupled to the processor means to receive timing configuration information, and having a first of the plurality of outputs being coupled to provide a processor timing signal to the processor means, a

second of the plurality of outputs being coupled to provide a latch timing signal to the data latch means, a third of the plurality of outputs being coupled to provide a control and voltage select logic circuit timing signal to the control and voltage select logic circuit, and a fourth of the plurality of outputs being coupled to provide a voltage select timing signal to the voltage select circuit.

11. A display driver in accordance with claim 10 further comprising a voltage generator means having an input coupled to the processor means for receiving voltage select configuration information, and for providing the corresponding plurality of input voltage levels to the voltage select circuit means in accordance with the voltage select configuration information.

12. A display driver in accordance with claim 11 further comprising an addressable register memory means coupled to the processor means for storing processor commands and status information communicated between the processor means and a host processor means, and for storing configuration information communicated from the host processor means.

13. A display driver comprising:

a memory having a data input coupled to receive pixel display data, an address input coupled to receive at least one address, and a pixel display data output coupled to provide the pixel display data;

a processor having a memory address output coupled to the address input of the memory, a display address output coupled to provide at least one display address, a pixel display data input coupled to the pixel data display output of the memory, and a pixel addressing data bits output; and

an addressable register having an address input coupled to the display address output of the processor, a pixel addressing data bits input coupled to the pixel addressing data bits output of the processor, and a pixel address data output,



wherein in a first mode of operation the processor stores the pixel display data at a storage location in the memory having the at least one address,

wherein in a second mode of operation the processor provides the at least one address to the memory to retrieve the pixel display data, and

wherein in a third mode of operation the processor provides the at least one display address and pixel addressing data bits to the addressable register memory.

14. A method for storing pixel display data in a display driver for a display, the method comprising the steps of:

a) receiving a display command and corresponding pixel display data;

b) storing the pixel display data in a memory in accordance with both the display command and a first predetermined addressing arrangement;

c) selectively retrieving the pixel display data from the memory in accordance with a second predetermined addressing arrangement;

d) processing the retrieved pixel display data for display in accordance with a predetermined display process to produce pixel addressing data bits;

e) storing the pixel addressing data bits in an addressable register in accordance with a third predetermined addressing arrangement, wherein the pixel addressing data bits are arranged in the addressable register to form at least one pixel address; and

f) providing the at least one pixel address at a pixel address data output for a display.

15. A method in accordance with claim 14 further comprising the steps of:

providing configuration information to the display driver; and



determining the first, second and third addressing arrangements from at least a portion of the configuration information.

16. A method in accordance with claim 14 wherein step (c) comprises the step of selectively retrieving the data from the memory in accordance with the first predetermined addressing arrangement.

17. A display driver comprising:

a processor means for storing pixel display data in a first memory in accordance with a first addressing arrangement, for selectively retrieving the pixel display data from the first memory in accordance with the first addressing arrangement, for processing the pixel display data to produce pixel addressing data bits, and for storing the pixel addressing display data bits in a second memory in accordance with a second addressing arrangement.