METHODS OF MANUFACTURING SEMICONDUCTOR STRUCTURES AND SEMICONDUCTOR STRUCTURES OBTAINED BY SUCH METHODS

FIELD OF THE INVENTION

The present invention relates to methods of manufacturing semiconductor devices in a substrate comprising a semi-conducting superficial layer arranged on an insulating layer, both of which are arranged on a partially exposed semi-conducting bulk region. The present invention also relates to substrates manufactured by such methods.

BACKGROUND OF THE INVENTION

Microelectronic devices are typically manufactured on either bulk semi-conductor substrates or on SOI substrates (Silicon on Insulator). It has also been proposed to use composite (or patterned) substrates comprising bulk areas and SOI areas. See, e.g., US patent 6,955,971. The fabrication of such patterned substrates is generally difficult because it requires formation of local areas of a buried oxide next to bulk areas. In the case of wafer bonding methods, such local oxide areas can be formed either on the top wafer or the base wafer, and can give rise to so-called "dishing" problems. In the case of a SIMOX type methods (Separation by Implanted Oxygen), such local oxide areas are commonly formed in the original wafer, but the differential thermal expansion of silicon oxides versus silicon gives rise to stress, etc.

SUMMARY OF THE INVENTION

The invention provides fabrication methods for patterned substrates having satisfactory crystalline quality, and the substrates fabricated by the provided methods.

In preferred embodiments, methods of the invention include providing a substrate comprising a semi-conducting support, a continuous insulating layer arranged on the support and a semi-conducting superficial layer arranged on the insulating layer; transforming the superficial layer and the insulating layer in at least one selected region of the substrate so as to form an exposed semi-conducting bulk region of the substrate; then forming electronic devices in or on the exposed semi-conducting bulk region of the substrate and in or on the superficial layer.

Substrates (or semiconductor structures) of the invention include a substrate comprising a semi-conducting support, an insulating layer disposed on a first face of the semi-conducting support and a semi-conducting superficial layer disposed on the insulating layer,

wherein the first face of the semi-conducting support comprises an exposed semi-conducting bulk region.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the invention will become apparent from the following description and the appended drawings:

Figs. 1 to 3 illustrate embodiments of the methods and substrates of the invention;

Figs. 4 and 5 illustrate further embodiments of the methods and substrates of the invention;

Fig. 6 illustrates another embodiment of a substrate of the invention;

Fig. 7 illustrates another embodiment of a substrate the invention;

Figs. 8 to 11 illustrate embodiments of lithography steps of the invention; and

Fig. 12 illustrates an embodiment of an etching step of the invention; and

Fig. 13 illustrates an embodiment of an implantation step of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The preferred embodiments and particular examples described herein should be seen as examples of the scope of the invention, but not as limiting the present invention. The scope of the present invention should be determined with reference to the claims.

Figure 1 illustrates an exemplary substrate useful for fabricating the invention. Here, the illustrated SOI substrate (silicon on insulator) comprises semi-conducting bulk support 1, continuous insulating layer 2 arranged on support 1, and semi-conducting superficial layer 3 arranged on insulating layer 2. Insulating layer 2 has a thickness preferably less than 25 nm (nano-meter), and more preferably between 2 nm and 25 nm. Superficial layer 3 has a thickness preferably between 5 nm and 50 nm, and more preferably between 12 nm and 20 nm for planar full depletion SOI transistors, or between 20 nm and 50 nm for vertical multiple gate transistors.

Figure 2 illustrates preferred embodiments of the substrates and methods of the invention. Here, the illustrated substrate (semi-conductor structure) comprises semi-conducting support 1, insulating layer 2 disposed on a region of first face 16 of semi-conducting support 1, and semi-conducting superficial layer 3 disposed on insulating layer 2. Another region of the first face 16 of semi-conducting support 1 includes exposed semi-conducting bulk region 12.

Methods of these embodiments comprise providing a substrate of Figure 1, and then transforming the substrate to form exposed semi-conducting bulk region 12 of the substrate. The word "transformed" is used herein to refer to the result of a process applied to one or more layers of a semiconductor structure, e.g., to the removal of the "transformed layers". In particular, here superficial layer 3 and insulating layer 2 are transformed by removal in selected region 4 of the substrate so as to form exposed semi-conducting bulk region 12 of support 1. These layers can be removed e.g. by an etching process that halts at support 1, and during which region 5 complementary to selected region 4 can be protected by a mask.

Figure 3 then illustrates that electronic devices 6 can be formed in (or on) exposed semi-conducting bulk region 12 and in (or on) superficial layer 3 of the substrate of Figure 2. Advantageously, the devices can be formed in the course of a single device forming process (a single sequence of steps), that is the devices are formed "at the same time" or "simultaneously" because their formation shares common steps. For example, only a single lithographic exposure can be performed for the devices in both regions, if the height offset between the surface of exposed semi-conducting bulk region 12 of the substrate and the surface of superficial layer 3 is less than the depth of focus of a lithography exposure (made by an image forming apparatus) corresponding to a predetermined image resolution. In that case, the images formed on exposed semi-conducting bulk region 12 and the images formed on superficial layer 3 have, at least, the predetermined image resolution and are suitable for forming the devices.

Support 1 and semi-conducting superficial layer 3 can comprise the same semi-conducting material, or different semi-conducting materials, or the same or different semi-conducting materials with different crystalline orientations. Electronic devices 6 formed respectively in exposed semi-conducting bulk region 12 of the substrate and in superficial layer 3 can be thus formed in different materials. The preferable semi-conducting materials for support 1 and superficial layer 3 are e.g. silicon, germanium, silicon-germanium, or III-V-type semi-conducting materials such as InP, GaN, or GaAs, optionally in a strained state. For instance, germanium could be chosen for PMOS transistors, and III-V-type semi-conducting materials for NMOS transistors, whereas silicon can be used for input-output-circuits and analog circuits.

Figure 4 illustrates further preferred embodiments of the substrates and methods of the invention. Here, the step of transforming superficial layer 3 and insulating layer 2 of a substrate of Figure 1 comprises *in situ* dissolution of insulating layer 2 in at least selected

region 4 of the substrate forming resulting layer 7. Resulting layer 7 has exposed semi-conducting region 12 that is contiguous with, or in electrical communication with, semi-conducting bulk support 1. In this embodiment, insulating layer 2 preferably comprises silicon oxide, dissolution of the oxide layer causes oxygen to diffuse from insulating layer 2, and due to the loss of oxygen in the insulation layer, resulting layer 7 is thinner than initial stack of layers 2 and 3.

Figure 5 illustrates that electronic devices 6 can be formed in (or on) exposed semi-conducting surface region 12 and in (or on) superficial layer 3 of the substrate of Figure 4. As in the previous embodiment, the height offset between the surface of exposed semi-conducting bulk region 12 of the substrate and surface of superficial layer 3 is preferably less than the depth of focus of a lithography exposure corresponding to a predetermined image resolution. Then, the devices can then be formed simultaneously, that is during the course of a single device forming process in which a single lithographic exposure is performed for devices in exposed semi-conducting surface region 12 and in superficial layer 3.

Figure 6 illustrates another exemplary substrate useful for fabricating the invention. Here, support 1 comprises epitaxial layer 14 on the surface of the support and with a density of crystalline defects of size greater than approximately 10 nm of preferably less than approximately $10^3/cm^3$. In particular, epitaxial surface layer 14 may be used for burying defects in the lower part of support 1, that may then have a density of crystalline defects of a size greater than approximately 10 nm of more than $10^3/cm^3$ or more than $10^5/cm^3$. Epitaxial surface layer 14 preferably has a thickness of, e.g., 0.1 micron or more.

Figure 7 illustrates further preferred embodiments of the substrates and methods of the invention. Here, the substrate comprises additional insulating layer 10 disposed on additional selected region 15 of superficial layer 3 and additional semi-conducting superficial layer 11 disposed on additional insulating layer 10.

A substrate with additional insulating layer 10 and additional semi-conducting superficial layer 11 is preferably manufactured by a SmartCut™. Then the following four layers are then removed in selected region 4 of the substrate: additional insulating layer 10, additional semi-conducting superficial layer 11, superficial layer 3 and insulating layer 2. In region 5 only additional insulating layer 10 and additional semi-conducting superficial layer 11 are removed. No layers are removed from additional selected region 15 so that electronic devices can be formed therein.

Generally, devices 6 (e.g., in Figs. 3, 5, and 7) can be formed by processes comprising a lithographic step or steps typically followed by an etching step or steps and/or an implantation step or steps. For the substrate of Figure 7, electronic devices 6 can then formed in (or on) exposed semi-conducting bulk region 12 of the substrate (region 4), and/or in (or on) superficial layer 3b (region 5), and/or in (or on) additional superficial layer 11 (region 15). The devices can be formed simultaneously, as is preferred, or sequentially.

Figure 8 illustrates a preferred lithography step according to the methods of the invention. Radiation, arrows 13, emanates from image forming apparatus 8 and impinges simultaneously on selected portions of exposed semi-conducting bulk region 12 of the substrate and on selected portions of superficial layer 3.

Height offset 9, the distance between the surface of exposed semi-conducting bulk region 12 of the substrate and the surface of superficial layer 3, is preferably less than the depth of focus of a lithography exposure corresponding to a predetermined image resolution made by image forming apparatus 8 along an axis Z. Therefore, a single lithography exposure can be sufficiently focused to at least the predetermined image resolution simultaneously on both exposed semi-conducting bulk region 12 of the substrate and on superficial layer 3. Accordingly, for formation of electronic devices in (or on) both of these regions, it is possible and advantageous either to carry out a single lithographic exposure or to carry out simultaneously two lithographic exposures. The depth of focus depends on the image forming apparatus used and on the resolution required by the process applied.

Height offset 9 is preferably less than the depth of focus of the selected lithography tool while taking into account the required image resolution for forming the smallest pattern. Specifically, height offset 9 is preferably less than 100 nm, or more preferably less than 50 nm. Indeed, when a higher precision is needed for small structures, e.g., for short gate lengths, the depth of focus is preferably also small and the height offset should thus preferably be no larger than the depth of focus. When a lower precision is suitable, a height offset of less than 100 nm might be sufficient.

For example, Figure 2 illustrates an embodiment in which the height offset corresponds to the combined thicknesses of superficial layer 3 and insulating layer 2. Hence, when using superficial layer 3 having a thickness of 20 nm or less and insulating layer 2 having a thickness of 25 nm or less, the combined thickness of both layers is 45 nm or less which is smaller than a preferred depth of focus of 50 nm, which is typical for current lithography techniques. Figure 4 illustrates an embodiment in which the height offset

corresponds to the difference between the combined thicknesses of superficial layer 3 and insulating layer 2 and the thickness of layer 7.

Figure 7 illustrates an embodiment in which a first height offset corresponds to the combined thicknesses of layers 2 and 3, and a second height offset corresponds to the combined thicknesses of layers 10 and 11; either one of both of these heights offsets, or the sum of both height offsets can be less than depth of focus of the selected lithography tool while taking into account the required image resolution for forming the smallest pattern.

Figure 9 illustrates another preferred lithography step according to the methods of the invention. In this embodiment, different types of electronic devices can be formed in exposed semi-conducting bulk region 12 and in superficial layer 3 (and also in additional superficial layer 11). The resolution required might be higher for one type of devices (e.g., devices formed on or in superficial layer 3) than for another type of devices (e.g., devices formed on or in bulk region 3). Then, smaller depth of focus 19a is suitable for the higher image resolution required for the devices in or on layer 3, while larger depth of focus 19b is suitable for the lower image resolution sufficient for devices in or on semi-conducting bulk region 12. Since larger depth of focus 19b is larger than, and overlaps, smaller depth of focus 19a, the lithography image on semi-conducting bulk region 12 is within its relevant depth of focus, depth of focus 19b at the same time as the lithography image on superficial layer 3 is within its relevant depth of focus, depth of focus 19a.

For example, memory devices can be formed in superficial layer 3 (and possibly in additional superficial layer 11 in Figure 7), and logic devices can be formed in semi-conducting bulk region 12, or conversely. Memory devices are typically smaller than logic devices and require higher lithographic image resolution than logic devices. The centre of focus of the lithography image forming apparatus is then preferably adjusted to the level where the smallest devices requiring the highest image resolution are to be formed, e.g. to superficial layer 3. Even if the other level (bulk region 12), is somewhat beyond the depth of focus (depth of focus 19a) corresponding to the smaller devices, one single lithography exposure can still be used if the other level (bulk region 12) is within a depth of focus (depth of focus 19b) corresponding to a lower image resolution sufficient for the larger devices.

This approach is not limited to the particular stacks of layers 1, 2, 3 and can also be implemented with any other substrates having several different levels, and in which electronic devices should be formed. This is for instance the case with a bulk substrate having two or more different surface levels.

Alternatively, two of more distinct lithography steps can be performed, especially when height offset 9 (Figure 9) is larger than the depth of focus of the image forming lithographic apparatus. Figures 10 and 11 illustrate such an embodiment. Figure 10 illustrates a first lithography step performed for exposed semi-conducting bulk region 12. Figure 11 illustrates a second lithography step performed for superficial layer 3 (see Figure 11).

Following the lithography step or steps, formation of electronic devices typically further comprises one or more etching steps and/or one or more implantation steps. In preferred embodiments, the etching steps, as shown by arrow 17 in Figure 12, are carried out simultaneously for both exposed semi-conducting bulk region 12 and superficial layer 3. In preferred embodiments, the implantation steps, as shown by arrow 18 in Figure 13, are also carried out simultaneously for both exposed semi-conducting bulk region 12 and superficial layer 3.

In particular, the etching and/or implantation steps are preferably carried out simultaneously in embodiments where insulating layer 2 has a thickness less than 25 nm (more preferably between 2 nm and 25 nm, and even more preferably between 5 nm and 15 nm), and where superficial layer 3 has a thickness preferably less than 50 nm (more preferably between 5 nm and 50 nm, and even more preferably between 10 nm and 40 nm). Prior lithography steps are preferably also carried out simultaneously when the above mentioned of depth of focus conditions are satisfied.

In other embodiments, distinct etching and/or distinct implantation steps can be carried out for exposed bulk region 12 and for superficial layer 3. In still other embodiments, the lithography, etching, and/or implantation can be carried out in any combination of separate and distinct or simultaneous steps for exposed semi-conducting bulk region 12 and superficial layer 3.

THE CLAIMS

What is claimed is:

1. A method of manufacturing a semiconductor device comprising:

providing a substrate comprising a semi-conducting bulk support, a continuous insulating layer arranged on the support, and a semi-conducting superficial layer arranged on the insulating layer;

transforming the superficial layer and the insulating layer so as to expose a selected region of the semi-conducting bulk support; and

simultaneously forming electronic devices in or on the exposed region of the support and in or on the superficial layer.

2. The method of claim 1 wherein the step of transforming comprises removing the superficial layer and the insulating layer in the selected region.

3. The method of claim 1 wherein the insulating layer comprises silicon oxide, and wherein the step of transforming comprises dissolution of the insulating layer in the selected region.

4. The method of claim 1 wherein the step of forming comprises a lithography step during which selected portions of the exposed semi-conducting bulk region and of the superficial layer are irradiated by an image forming apparatus.

5. The method of claim 4 wherein the image forming apparatus has a depth of focus along an axis perpendicular to the substrate that corresponds to a predetermined image resolution, and wherein a height offset between the exposed semi-conducting bulk region and the superficial layer is less than the depth of focus.

6. The method of claim 5 wherein the height offset is less than 50 nm.

7. The method of claim 5 wherein the height offset corresponds to a combined thickness of the superficial layer and the insulating layer.

8. The method of claim 4 wherein the step of forming further comprises:

etching of the exposed semi-conducting bulk region and the superficial layer; and

implanting into the exposed semi-conducting bulk region and the superficial layer.

9. The method of claim 1 wherein the semi-conducting bulk support comprises an epitaxial surface layer with a density of crystalline defects of a size greater than 10 nm of less than 10^3 /cm^3.

10. The method of claim 1 wherein the substrate further comprises an additional insulating layer disposed on a surface of the superficial layer so as to cover an additional selected region of the surface of the superficial layer while leaving exposed another region of the surface of the superficial layer and an additional semi-conducting superficial layer disposed on the additional insulating layer.

11. The method of claim 10 wherein forming further comprises forming electronic devices simultaneously in or on the exposed semi-conducting bulk region, the superficial layer, and the additional superficial layer.

12. A semiconductor a substrate structure comprising:

a semi-conducting bulk support;

an insulating layer disposed on a surface of the semi-conducting bulk support so as to cover a selected region of the surface of the semi-conducting bulk support while leaving exposed another region of the surface of the semi-conducting bulk support; and

a semi-conducting superficial layer disposed on the insulating layer.

13. The semiconductor structure of claim 12 further comprising electronic devices formed in the superficial layer and in the exposed region of the semi-conducting bulk support.

14. The semiconductor structure of claim 12 further comprising:

an additional insulating layer disposed on a surface of the superficial layer so as to cover an additional selected region of the surface of the superficial layer while leaving exposed another region of the surface of the superficial layer; and

an additional semi-conducting superficial layer disposed on the additional insulating layer.

15. The semiconductor structure of claim 14 further comprising electronic devices formed in the additional superficial layer, in the superficial layer, and in the exposed region of the semi-conducting bulk support.

16. The semiconductor structure of claim 12 wherein a combined thickness of the superficial layer and the insulating layer is less 50 nm.

17. The semiconductor structure of claim 12 wherein the semi-conducting support comprises an epitaxial surface layer with a density of crystalline defects of a size greater than 10 nm of less than $10^3/cm^3$.