

ABSTRACT**DIFFERENTIAL SENSE AMPLIFIER WITHOUT DEDICATED PRECHARGE
TRANSISTORS**

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Descriptive abstract

The invention A differential sense amplifier for sensing data stored in a plurality of memory cells (C) of a memory cell array, including:

- a first CMOS inverter having an output connected to a first bit line (BL) and an
10 input connected to a second bit line (/BL) complementary to the first bit line,
- a second CMOS inverter having an output connected to the second bit line (/BL) and an input connected to the first bit line (BL),

each CMOS inverter comprising a pull-up transistor (M21, M22) and a pull-down transistor (M31, M32), said sense amplifier having a pair of precharge transistors
15 arranged to be respectively coupled to said first and second bit lines (BL, /BL), so as to precharge said first and second bit lines (BL, /BL) to a precharge voltage, wherein said precharge transistors are constituted by the pull-up transistors (M21, M22) or by the pull-down transistors (M31, M32).

20 FIGURE 3