

1399 400

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO DISPLAY ARRANGEMENTS

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese company of 3-4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to display arrangements and to calculating apparatus incorporating the same. More specifically the invention relates to display arrangements wherein a display segment using a nematic-type liquid crystal in order to display figures, letters, symbols or the like is driven by alternating current voltage. The invention is especially and advantageously applicable to portable small-sized calculators and the like especially in cases in which the display has many columns.

Liquid crystals (nematic type crystals) will exhibit light scattering properties with very low consumption of electric power if voltages of the order of several volts to several tens of volts are applied thereto. If, however, the applied voltage is a direct current voltage, the electrodes of the crystal are apt to become stained and bubbles are apt to be generated in the liquid crystal. These effects cause marked deterioration of the quality of the display given by a liquid crystal display cell. Furthermore loss of resolution is apt to occur by action of the unidirectional current upon impurities in the liquid crystal and for other reasons which are not as yet fully understood beyond that the unidirectional flow of current is to blame. Indeed, with some known liquid crystals, such deterioration of the display and/or loss of resolution may occur after comparatively little use—for example after only several tens of hours of use. If, however, alternating current voltage—for example a sinusoidal or a rectangular wave of voltage—is applied to the liquid crystal, the current flowing through it is alternating instead of unidirectional, there is, in consequence, no generation of bubbles and no resolution of molecules, and the useful life of a liquid

crystal display cell can be expected to be much greater—several tens of thousands of hours so that, in this respect (satisfactory long useful life), a liquid crystal display cell becomes, practically speaking, as good as other forms of display cell e.g. those employing cold cathode gas discharge tubes, or fluorescent display tubes, or those with light emitting diodes.

However known circuit arrangements for producing an alternating current voltage drive to a liquid crystal display cell for such purposes as providing the display for a calculator, or a measuring equipment, have the defect of being undesirably complex and expensive, for the driving alternating current voltages must correspond with a data signal output (from the calculator or other equipment) and involve timing signals. Most conventional driving circuit arrangements for display cells which are not of the liquid crystal type—e.g. cold cathode gas discharge tube display cells—are dynamic in character.

Figure 1 of the accompanying drawings shows diagrammatically and so far as is necessary to an understanding thereof, a typical known driving circuit arrangement driving a display with display cells of the cold cathode gas discharge tube type.

Referring to Figure 1, in the arrangement therein represented, the display is given by a plurality of cold cathode gas discharge tube display cells arranged in rows and columns (only one row is shown). Timing impulses are applied, as at 1-a₁, 1-a₂, . . . 1-a_n (through transistors as shown) to the anodes in the columns. In each cell (i.e. tube) there is a plurality of co-planar cold cathodes and corresponding cold cathodes are connected in parallel for feeding with data signals applied (through transistors as shown) at 1-b₁, 1-b₂ . . . 1-b_n. Illumination is produced dynamically between a cold cathode and an anode when a timing signal occurs on an anode and a data signal occurs on a cold cathode simultaneously.

Figure 2 of the accompanying drawings

shows in generalised block diagram form a conventional driving circuit arrangement for a display comprising liquid crystal display cells in the block 2-g. In Figure 2 data input signals from a computing circuit are applied at terminals 2-c and block 2-f contains sets 2-d₁ . . . 2-d_n of memory circuits incorporating flip-flop circuits FF. Block 2-e represents a set of signal transforming circuits. An alternating driving signal is applied at 2-h. 2-d₁ . . . 2-d_n receive timing impulses as well as the data input signals and memorize the data signals to be displayed by the different cell display sections (between the common electrode of each cell and the different individual opposite electrodes associated therewith). In the transforming circuits of block 2-e, the signals memorized by the flip-flop circuits within the block 2-f are transformed into alternating current data signals, the alternating current voltage for actual driving of the liquid crystal cells being obtained from an alternating current voltage input applied at 2-h. In Figure 2 the gates incorporated in the block 2-e are conventionally represented and, as will be seen from the diagram, alternating current voltage is applied also to the common electrodes of the display cells. Corresponding opposed electrodes in the different cells are fed in parallel. All the electrodes are energised by alternating current voltage signals, the alternating current voltage being derived from 2-h. The data signals memorized in the flip-flop circuits in block 2-f are transformed into alternating current data signals by the signal transforming circuits in block 2-e. The alternating current voltage data signal applied to any opposed electrode has the same period as the alternating current voltage applied to the associated common electrode, but is of opposite instantaneous polarity if illumination is to occur between that opposite electrode and that common electrode. If illumination is not to occur between said opposed electrode and said common electrode, the two alternating current voltages applied are of the same instantaneous polarity i.e. they are in phase. Because the signal applied to an opposed electrode where illumination is to occur is in phase opposition to that applied to the associated common electrode the electric field between said opposed electrode and said common electrode will reverse at each half period of the applied alternating current voltage, and alternating current will flow in the appropriate part of the liquid crystal cell. Where illumination is not to occur said opposed electrode and said common electrode will always be at the same potential (since the applied voltages are in phase) and no current flows in the part of the cell in question.

Figure 2a shows diagrammatically and in more detail than Figure 2 part of the circuitry of the said Figure 2 the said Figure 2a showing the circuitry for only one of the display

elements incorporated in a liquid crystal display cell. In Figure 2a the said cell is shown broken away, the liquid crystal layer being represented by cross hatching at LQ. As will be apparent from Figure 2a the memory circuits in the block 2-f (Figure 2: represented under the bracket 2-f in Figure 2a) and the signal transforming circuits in the block 2e (Figure 2: represented under the bracket 2-e in Figure 2a) employ P-channel MOSFETS as their active elements. As will also be apparent the operating voltage of the liquid crystal display cell (under the bracket Figure 2-g in Figure 2a) is equal to the circuit operating voltage V_{DD}. An known circuit arrangement as illustrated in Figures 2 and 2a is suitable for driving a liquid crystal display in accordance with data output signals from, for example, a calculator, measuring equipment or machine monitoring equipment but it will be seen that it involves the provision of a substantial number of flip-flop circuits and a complex arrangement of numerous gates. The number of circuit elements—flip-flops and gates—is therefore very substantial indeed and the arrangement is thus undesirably complex and expensive. The alternating signal at 2-h is normally a rectangular wave with a duty ratio of 1:2 and a frequency of the order of several tens Hz to several hundreds Hz.

The arrangement of Figures 2 and 2a is thus not suited, on grounds of cost, for measuring equipment and the present invention seeks to provide a considerably simpler and cheaper driving circuit arrangement suitable for providing alternating current voltage drive for the liquid crystal display of such an apparatus.

According to one aspect of the present invention there is provided a display arrangement comprising a plurality of liquid crystal display segments arranged in at least one column, the display segments of the column or at least one of the columns having a common electrode, and a driving circuit arrangement comprising transforming circuits for transforming input data signals into alternating current voltage data signals of uniform period and memory circuits for memorising the alternating current voltage data signals and for supplying respective alternating current voltage data signals to each segment under the control of timing pulses, the arrangement being such that a given display segment produces a display upon receipt of an output signal from said memory circuits and an alternating current voltage output signal on the common electrode of the column or columns.

Preferably, the arrangement is such that the period of the alternating current voltage data signals is greater than the period of the timing pulses.

There may be provided means for synchronising the alternating current voltage out-

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put signal on the common electrode of the column or columns with the output signals sent to associated opposed electrodes of the display segments from the memory circuits, said means including a gate circuit.

In one of its most important practical applications the invention provides calculators, for example portable small sized calculators, having a display arrangement as just set forth.

Figure 3 of the accompanying drawings shows, in block diagram form the general arrangement of one embodiment of this invention. Referring to Figure 3, data input signals from, for example, a calculator, are applied to terminals 3-c. In circuit block 3-e the input data signals are transformed into alternating current voltage data signals, an alternating current voltage signal being applied from a terminal 3-h to the gates shown in the block 3-e, the input data signals being inverted at the period T_2 of the alternating current voltage signal applied at terminal 3-h. Timing signals are applied at terminals

3-d₁ . . . 3-d_n of a memory circuit block 3-f to which the alternating current voltage data signals from block 3-e are also applied as shown. The output signal from the block 3-f is fed to a plurality of liquid crystal display segments arranged in one or more columns 3g. Figure 3a, the relation of which to Figure 3 is of the same general nature as the relation of Figure 2a to Figure 2, is a diagram showing, in more detail, part of the circuitry of Figure 3. In Figure 3a (as in Figure 2a) the display segments are shown broken away, the liquid crystal layer being represented by cross hatching at LQ. As will be seen the active elements of the blocks 3-e, 3-f (under brackets in Figure 3a) are P-channel MOSFETS. In block 3-f of Figure 3 is a matrix of memory circuits for the alternating current voltage data signals. In this matrix there are, as shown in the accompanying Figure 5, two transistors, employed for each memory circuit corresponding to each display segment. The structure of this matrix is thus very simple. In Figure 5 alternating current voltage data signals from the block 3-e appear at terminals 5-c₁, 5-c₂. The gates represented in the block 3-e constitute exclusive -OR logic circuits and each may be constituted by a combination of two transistors as shown in the accompanying Figure 4. In Figure 4 the transistors employed are, as already stated, of the P-channel MOSFET type and are connected to constitute an exclusive OR logic circuit with terminals 4-o, 4-i₁ and 4-i₂ as shown.

The number of elements in the block 3-e represented in Figure 3 and 3a is equal to the number of display segments in one column regardless of the number of columns. Also, the number of elements in the block 3-f is reduced by replacing the conventional flip-flop circuits of Figure 2 provided for each display

segment with the matrix of memory circuits in the block 3-f in Figures 3 and 3a. In each memory circuit, use is made of the capacity of the gate electrode of a transistor on the side of the output signal. In a normal small sized table calculator, the alternating current voltage data signals appearing at terminals 5c₁, 5c₂ (see Figure 5) exists at several hundreds Hz to several KHz. For an output stage transistor for driving each display segment and for driving the common electrode, it is desirable to use a complementary type of circuit as shown at 3-j of Figure 3 or a circuit similar to this. By this means an alternating current voltage output signal is applied to the common electrode. As, however, the resistance value of a liquid crystal display segment is extremely high (some reach to several hundreds MΩ), it is satisfactory simply to insert a sufficiently small resistance on one side for the resistance value of a display segment instead of using a transistor here. The resistance value of the side of the common electrode is chosen sufficiently smaller than the resistance value of all the segments being parallel.

As regards the alternating current voltage signal for driving the display, the period T_2 thereof is preferably greater than the circulating period T_1 of the timing signals. Normally, it is desirable to choose the period T_2 several times as large as the period T_1 .

Figure 6 of the accompanying drawings, is an explanatory graphical figure. Here signal A represents timing pulses applied to terminals 3-d₁ . . . 3-d_n, signal B represents the alternating current voltage signal applied to the terminal 3-h and signal C shows the lag of the timing pulses A with respect to the inversion point of the signal B. Signal B is inverted at time t_1 , but signal A is inverted at time t_2 . Accordingly between the inversion at time t_1 of the electric potential on the side of the common electrode and the inversion at time t_2 of the electric potential at an opposed (segment) electrode (the output signal from the memory circuit), there occurs the time difference Δt_1 . This is given by

$$\Delta t_1 = t_2 - t_1 (\Delta t_n = t_{2n} - t_{2n-1}) < T_1$$

This inevitably occurs if the periods of the signals A and B are not synchronised. If the above-described Δt_n is chosen sufficiently smaller than $T_2/2$, the time difference Δt causes no problem because the lag of response of a liquid crystal display segment is large and because the frequency of the signal B is chosen above the frequency to which human eyesight can respond. Normally, it is simple to select signal A more than several hundreds Hz and signal B about several tens Hz.

If, in any particular case it is necessary to choose the frequency of the alternating current voltage data signals less than several hundred

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Hz, or to choose the frequency of the signal B near the frequency of the alternating current voltage data signals, Δt may be about $T_2/2$. In such a case, Δt should be made zero by synchronizing the periods T_1 and T_2 . If a synchronizing circuit is not provided then as shown in the accompanying Figure 7, the signal on an opposed (segment) electrode can be easily synchronized with the signal from the common electrode by providing the or each common electrode of the display segments with a single transistor for controlling a gate in accordance with the timing signal to the terminal 3-d.

As will now be seen, from Figures 3 and 3a the circuits for connecting the data input signal with the alternating current voltage signal for driving the display segments are not under the control of the number of columns. Accordingly circuits for connecting with the timing signals are not needed, the data input signals (from, for example, a computing circuit) being merely fed to the block 3-f after transformation into the alternating current voltage data signals inverted at the half period of the alternating current voltage signal. There is therefore a substantial reduction in the number of circuits necessary, as compared with a known arrangement as represented in Figure 2 for the illumination in each display segment is obtained as required without having to provide an alternating drive circuit for each display segment of each column. Further the period T_2 of the alternating current voltage signal can normally be selected at a value between limits well above the period T_1 , so that it is unnecessary to synchronize the two signals concerned. The advantages of alternating current voltage drive to a liquid crystal display are obtained; driving voltages well above the threshold voltage necessary to cause illumination of the crystal are readily obtainable; and the relatively slow response of a liquid crystal does not cause difficulties.

WHAT WE CLAIM IS:—

1. A display arrangement comprising a plurality of liquid crystal display segments arranged in at least one column, the display segments of the column or at least one of the columns having a common electrode, and a driving circuit arrangement comprising transforming circuits for transforming input data signals into alternating current voltage data signals of uniform period and memory circuits for memorizing the alternating current voltage data signals and for supplying respective altering current voltage data signals to each segment under the control of timing pulses, the arrangement being such that a given display segment produces a display upon receipt of an output signal from said memory circuits and an alternating current voltage output signal on the common electrode of the column or columns.

2. An arrangement as claimed in claim 1 wherein the arrangement is such that the period of the alternating current voltage data signals is greater than the period of the timing pulses.

3. An arrangement as claimed in claim 1 or 2 and comprising means for synchronising the alternating current voltage output signal on the common electrode of the column or columns with the output signals sent to associated opposed electrodes of the display segments from the memory circuits, said means including a gate circuit.

4. A display arrangement substantially as herein described with reference to Figures 3 to 7 of the accompanying drawings.

5. Calculating apparatus having a display arrangement as claimed in any of claims 1 to 4.

J. MILLER & CO.,
Agents for the Applicants,
Chartered Patent Agents,
262 High Holborn,
London, WC1V 7EP.

Hz, or to choose the frequency of the signal B near the frequency of the alternating current voltage data signals, Δt may be about $T_2/2$. In such a case, Δt should be made zero by synchronizing the periods T_1 and T_2 . If a synchronizing circuit is not provided then as shown in the accompanying Figure 7, the signal on an opposed (segment) electrode can be easily synchronized with the signal from the common electrode by providing the or each common electrode of the display segments with a single transistor for controlling a gate in accordance with the timing signal to the terminal 3-d.

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2. An arrangement as claimed in claim 1 wherein the arrangement is such that the period of the alternating current voltage data signals is greater than the period of the timing pulses.
3. An arrangement as claimed in claim 1 or 2 and comprising means for synchronising the alternating current voltage output signal on the common electrode of the column or columns with the output signals sent to associated opposed electrodes of the display segments from the memory circuits, said means including a gate circuit.
4. A display arrangement substantially as herein described with reference to Figures 3 to 7 of the accompanying drawings.
5. Calculating apparatus having a display arrangement as claimed in any of claims 1 to 4.

J. MILLER & CO.,
Agents for the Applicants,
Chartered Patent Agents,
262 High Holborn,
London, WC1V 7EF.

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