

FIG. 1

$$H=\begin{array}{c} \begin{matrix} V_1 & V_2 & V_3 & V_4 & V_5 & V_6 & V_7 & V_8 \end{matrix} \\ \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix} \end{array} \begin{matrix} C_1 \\ C_2 \\ C_3 \\ C_4 \end{matrix}$$

FIG. 2A

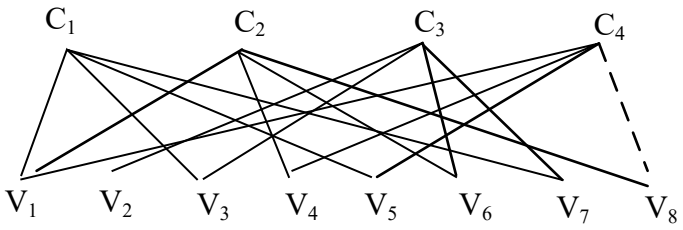


FIG. 2B

13	48	80	66	4	74	7	30	76	52	37	60	−	49	73	31	74	73	23	−	1	0	−	−
69	63	74	56	64	77	57	65	6	16	51	−	64	−	68	9	48	62	54	27	−	0	0	−
51	15	0	80	24	25	42	54	44	71	71	9	67	35	−	58	−	29	−	53	0	−	0	0
16	29	36	41	44	56	59	37	50	24	−	65	4	65	52	−	4	−	73	52	1	−	−	0

FIG. 3A

$$\begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \\ 1 & 0 & 0 & \cdots & 0 \end{bmatrix}$$

FIG. 3B

Step 1: Determine to-be-coded data bits, such as payload bits (payload bits)

Step 2: Determine a length of an LDPC codeword and a number of codewords, so as to determine the LDPC codeword

Step 3: Perform a shortening operation on the to-be-coded data bits, to be specific, fill in shortening zero bits (shortening zero bits) after the to-be-coded data bits

Step 4: Encode to-be-coded data bits and shortening zero bits in each LDPC codeword by using an LDPC code parity-check matrix to generate parity bits (Parity bits), and then delete the shortening zero bits

Step 5: Repeat (repeat) some to-be-coded data bits in the LDPC codeword, or puncture (puncture) the parity bits in the LDPC codeword, so that processed (punctured or repeated) codeword bits exactly fill an OFDM symbol to be transmitted to

Step 6: Concatenate (concatenation) a plurality of codewords and perform stream parsing (stream parsing)


Payload bits (payload bits)


Shortening zero bits (shortening zero bits)


Parity bits (Parity bits)


Repeat bits (repeat bits)

Punch

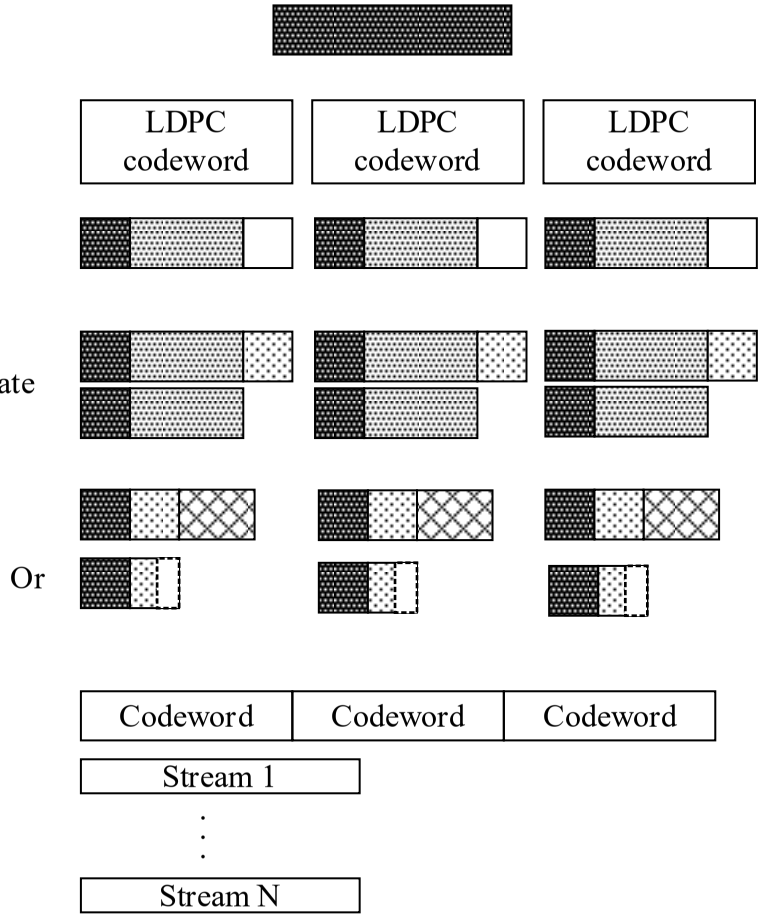


FIG. 4

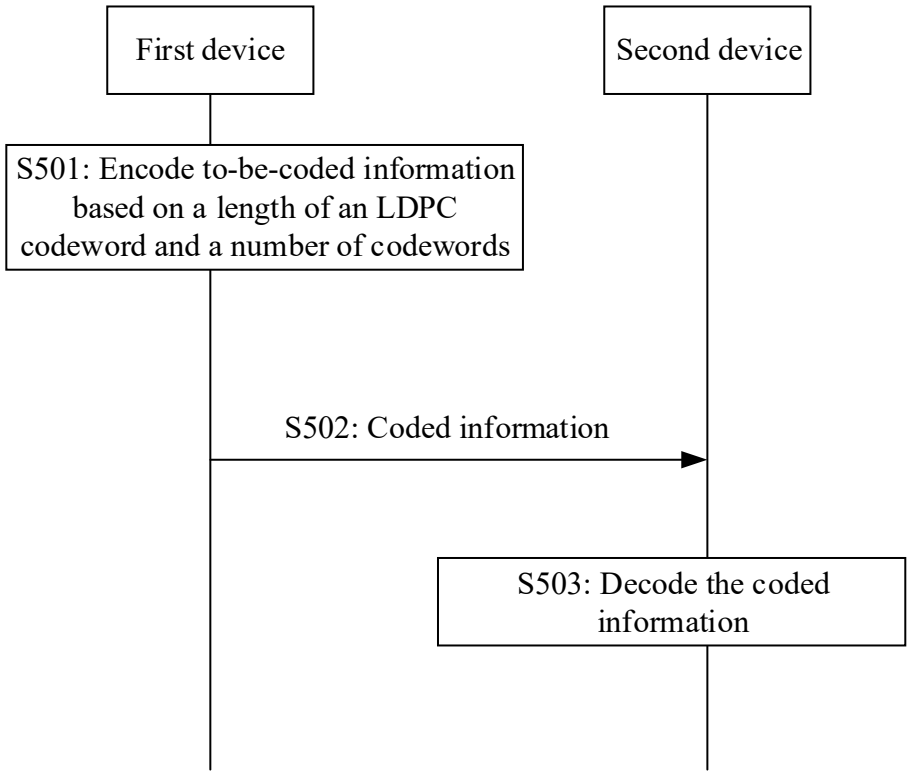

First device
Second device
S501: Encode to-be-coded information based on a length of an LDPC codeword and a number of codewords
S502: Coded information
S503: Decode the coded information

FIG. 5

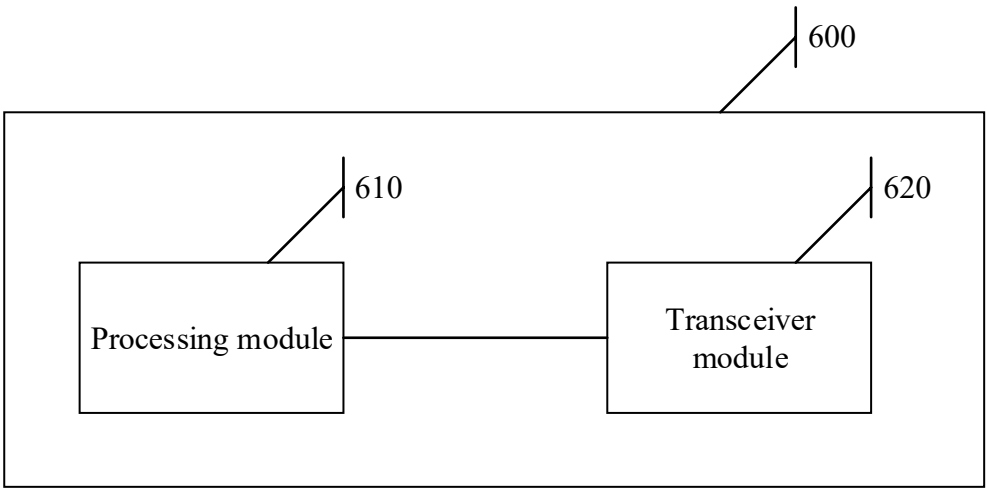

600
610
620
Processing module
Transceiver module

FIG. 6

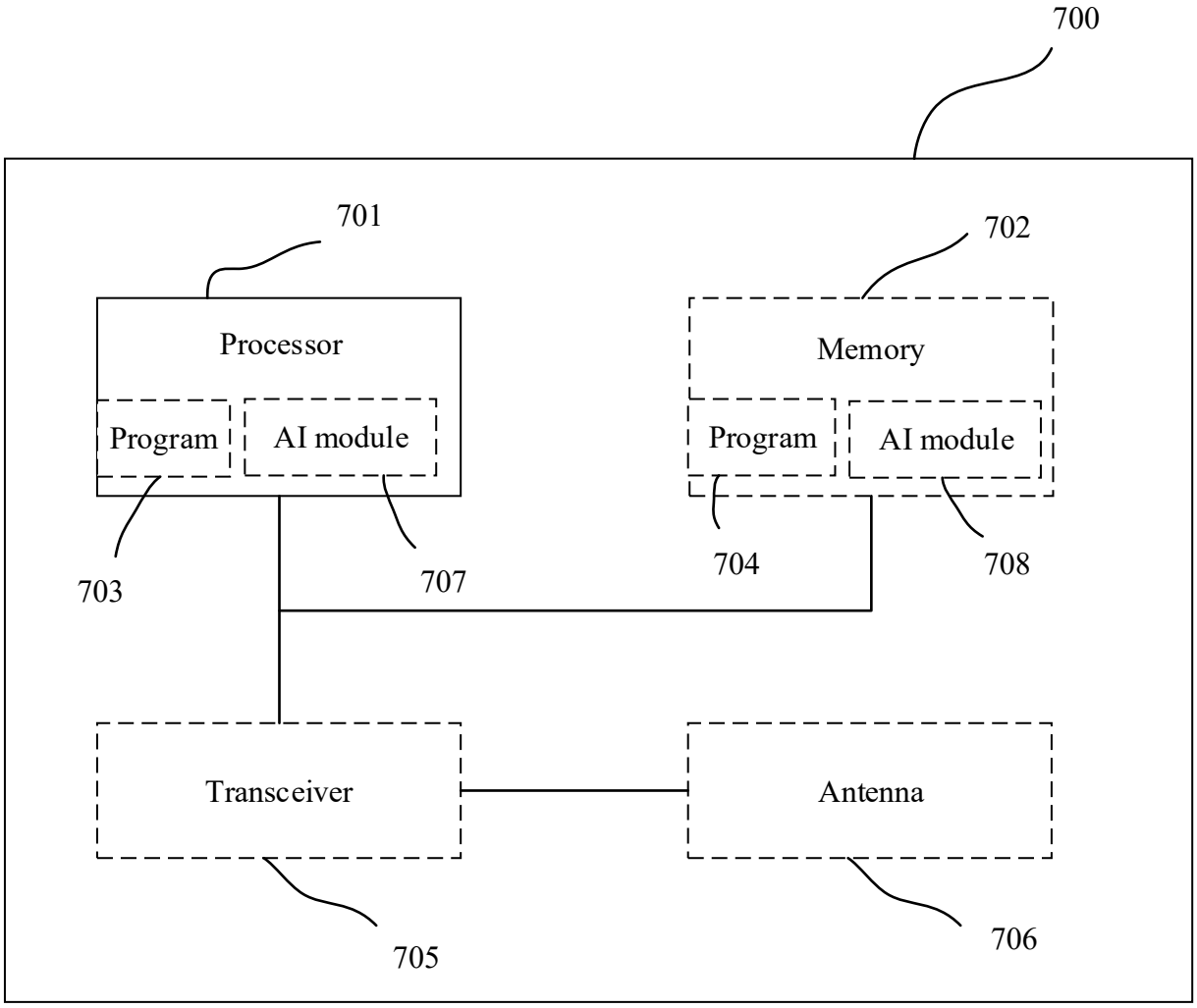

700
701
Processor
Program
AI module
703
707
702
Memory
Program
AI module
704
708
Transceiver
Antenna
705
706

FIG. 7