

PROCESS FOR MANUFACTURING A MULTILAYER STRUCTURE MADE FROM
SEMICONDUCTING MATERIALS

This invention relates to a process for manufacturing a multilayer structure made from semiconducting materials and comprising an active layer, a support layer and an electrically insulating layer between the active layer and
5 the support layer.

The invention also relates to structures obtained using such a process.

Note that the invention is applicable to thin structures in the form of wafers, of the type used for
10 microelectronics, optical and optronic applications.

In the remainder of this text, the general expression "structure concerned by the invention" will be used to denote a structure like that mentioned above, of the multilayer structure type made from semiconducting
15 materials and comprising an active layer, a support layer and an electrically insulating layer between the active layer and the support layer.

The multilayer structures combine several layers, some of which are made from different materials.

Thus, one application of the invention is the manufacture of SOI (Silicon On Insulator) type structures.

5 An SOI of this type thus usually comprises:

- an active layer made from monocrystalline silicon with a low resistivity (of the order of a few Ohms.cm),
- a support layer may be made of silicon with a significantly higher resistivity, typically more than
10 1000 Ohms.cm,
- and an electrically insulating layer between these two layers, for example an SiO₂ layer.

The so-called "active" layer is named this way because components will be placed on it, typically electronic or
15 optronic components.

It is desired that the multilayer structures concerned by the invention are associated with the lowest possible electrical losses.

Note that in this text, "losses" refers to electrical
20 losses in the structure support layer, the said losses originating from polarised operation of the components made on the active layer.

These losses are disadvantageous, to the extent that they affect the electrical efficiency of this structure and
25 can generate noise affecting the signal quality in the active layer (particularly for very high frequency applications - in other words for frequencies typically more than 10 GHz).

Thus, structures to which embodiments of the invention are applicable usually have:

- a low electrical resistivity (of the order of 5 to 30 Ω .cm) at their active layer, to enable good
5 interaction of components installed on this layer,

- and a much higher resistivity at the layers that support this active layer, to avoid electrical losses in the structure. To achieve this, the support layer in a structure concerned by the invention (typically, but not
10 necessarily an SOI) will typically have a much higher resistivity than the active layer (for example more than 1000 Ω .cm).

The high resistivity of layers supporting the active layer of these structures is thus designed to reduce losses
15 associated with the structure.

Embodiments of this invention seek to make structures of the type mentioned at the beginning of this text, in which losses are as low as possible.

And note that in very high frequency applications,
20 electrical signals generated in the active layer of the structure can pass through the insulating layer of the structure despite the electrical insulation effect of this layer. This corresponds to losses that are undesirable, as mentioned above.

25 Thus, and even more precisely than as described above, another purpose of the invention is to be able to make structures like those mentioned above in which losses are minimised, and this also for very high frequency applications.

A first aspect of the invention provides a process for manufacturing a multilayer structure made from semiconducting materials and comprising an active layer, a support layer and an electrically insulating layer between the active layer and the support layer, characterised in that the process comprises modification of the density of carrier traps and / or the electrical charge within the electrically insulating layer, in order to minimise electrical losses in the structure support layer.

Other preferred but non-limitative embodiments of such a process are as follows:

- the said modification may be intended to increase the density of carrier traps at the interface between the structure insulating layer and the structure support layer,
- the said modification may be designed to reduce the electrical charge within the electrically insulating layer of the structure,
- the active layer may be chosen so as to have a much lower resistivity than the support layer,
- the process may include bonding of a first substrate comprising the structure active layer and a second substrate comprising the structure support layer,
- the said first substrate may comprise an insulating layer;
- the said insulating layer of the first substrate may correspond to the insulating layer of the structure,
- in order to minimise electrical losses in the structure support layer, the density of the carrier traps

may be modified before the said first substrate and the said second substrate are bonded,

- in order to minimise electrical losses in the structure support layer, the density of the carrier traps
5 may be modified by inserting an intermediate layer between the said two substrates to be bonded, that may come into contact with the support layer of the second substrate, the material of the said intermediate layer being chosen so as to increase the density of the carrier traps, due to its
10 association with the material in the said support layer,

- the said intermediate layer may be deposited on the said second substrate, before the said bonding of the first and second substrates,

- the said support layer may be made of silicon and
15 the material used in the said intermediate layer may be a nitrided oxide,

- the density of carrier traps may be modified using at least one material that tends to increase the density of carrier traps due to its association with the
20 material in the said support layer, for bonding the said first and second substrates, to minimise electrical losses in the structure support layer,

- the density of carrier traps may be modified by applying a treatment to the surface region of the second
25 substrate before the said first and second substrates are bonded, in order to minimise electrical losses in the structure support layer,

- the said treatment of the surface region of the second substrate may include controlled deterioration of the surface condition of the second substrate,

- in order to minimise electrical losses within the structure support layer, the charge may be modified in the electrically insulating layer by adjusting the characteristics of an implantation made in the said first substrate before the said first and second substrates are bonded,

- the doses of the said implantation may be adjusted to modify the charge in the electrically insulating layer,

- the said implantation may correspond to a weakening implantation of a SMARTCUT® type process,

- in order to minimize electrical losses in the structure support layer, the charge within the electrically insulating layer may be modified by adjusting the parameters of a thermal oxidation made on the said first substrate to create the structure insulating layer on its surface,

- the said parameters may include the temperature and / or temperature variation, the gas composition, annealing times, etc.

- the charge within the electrically insulating layer can be modified by adjusting the parameters of a heat treatment that is applied to the said structure once the structure has been formed, in order to minimise electrical losses in the structure support layer,

- the thermal budget of the said heat treatment may be adjusted so as to reduce the charge within the electrically insulating layer of the structure,

- the said structure may be is an SOI,
- the process may use steps in a SMARTCUT® type process.

Other aspects, purposes and advantages of the invention will become clear after reading the following description of the invention with reference to the attached drawings in which:

• Figure 1 is a graph derived from simulations, illustrating the variation of a parameter G_{EFF} representing losses associated with the structure as a function of different corresponding values of the electrical charge of the insulating layer, for different structures concerned by the invention,

• Figure 2 is a graph of the same type like that illustrated in Figure 1, also derived from simulations, illustrating the variation of the same parameter G_{EFF} representing losses associated with the structure as a function of the different corresponding values of the density of carrier traps at the interface between the insulating layer and the support layer, for different structures concerned by the invention,

• Figure 3 is a diagram illustrating the principle of a method for measuring electrical losses in a structure such as structures concerned by the invention, the said structure being shown in a sectional view, and the right part of the diagram containing a representation of an equivalent electrical circuit,

• Figure 4 is a graph derived from experimental measurements and illustrating the influence of a reduction

in the density of carrier traps at the interface between the insulating layer and the structure support layer concerned by the invention, on electrical losses measured for a structure concerned by the invention,

5 • Figure 5 is a graph of the same type as that shown in Figure 4, also derived from experimental measurements, illustrating the influence of a modification to the charge within the electrically insulating layer of the structure concerned by the invention on the electrical
10 losses measured for this structure,

 • Figure 6 diagrammatically illustrates bonding of two substrates to constitute a structure concerned by the invention, at least one of the two substrates having been specifically treated according to one of the embodiments of
15 the invention in order to minimise losses associated with the structure that will be obtained,

 • Figure 7 represents measured losses as a function of the frequency, for different structures with different values for the parameters Q_{Box} and D_{it} .

20 We will now describe several embodiments of the invention for a multilayer structure like that mentioned in the introduction to this text.

 Note that this structure may in particular be an SOI type structure (although this is not limitative).

25 In general, the structures concerned by the invention are typically structures in which the electrical resistivity of the active layer is significantly lower than the resistivity of the structure support layer.

Note also that the process that will be described below may be used in the more general context of implementation of a SMARTCUT® type process for manufacturing the multilayer structure.

5 However, it is quite possible that the process according to the invention could be implemented in the general context of processes for manufacturing multilayer structures different from the SMARTCUT® process.

10 In particular, the process can be used in the general context of a process for making a multilayer structure implementing a step to bond two substrates, and different from the SMARTCUT® process (for example ELTRAN type process, etc.)

15 Using an SOI type structure example as an illustration, the invention modifies:

- the charge within the electrically insulating layer of the structure,
 - and / or the density of the carrier traps (typically at the interface between the insulating layer and the structure support layer),
- 20 in order to minimise losses associated with this structure.

The applicants have indeed determined, after carrying out simulations and experimental observations, that it is possible to reduce losses associated with the structure by:

- reducing the electrical charge within the electrically insulating layer of the structure. In this respect, the applicants used the demonstration of how losses are influenced by the value of the parameter Q_{BOX} ,

that corresponds to the electrical charge associated with the insulating layer of the structure (in other words the buried oxide layer in the case of an SOI).

• and / or increasing the density of carrier traps, more particularly at the interface between the insulating layer of the structure and its support layer. In this respect, the applicants used the demonstration of how losses are influenced by the value of the parameter D_{it} that corresponds to the density of carrier traps.

In order to avoid any confusion, it is specified that the "carrier traps" (or "carriers") which are referred to are electrical traps which aim at trapping electrical charges which have been put into motion by fixed charges present in the structure. In this respect, the carrier traps are in particular distinct from gettering means which aim at gettering elements such as physical impurities (such impurities can be e.g. metallic ions, for example from heavy metals, etc...).

The present invention uses the demonstration of the two influences mentioned above, namely the values of parameters D_{it} and Q_{BOX} .

And as a follow up to this demonstration, the applicants carried out a series of observations on different structures of the type mentioned above, and concerned by the invention.

These observations were thus related to different structures to which the different values of the parameters D_{it} and Q_{BOX} were associated, and for which losses were measured.

More precisely, the applicants selectively modified the following for each of these structures:

- firstly, the electrical charge in the insulating layer of the structure,

- secondly, the carrier density at the interface between the insulating layer and the structure support layer.

We will discuss means of making these modifications in more detail.

Before presenting the results of numerical simulations and of experiments carried out by the applicants, we will briefly summarise the principles involved in a method of measuring losses used in the context of these simulations and experiments.

This loss measurement method is usually called loss measurement by coplanar lines.

It provides a means of measuring losses up to a certain depth as a function of spreading of electromagnetic fields in the support layer. This depth depends on the spacing between conductors, the frequency and resistivity of the support layer and the oxide thickness.

This measurement method thus uses the following steps for each structure to be characterised:

- Structure preparation, by:

- Selective etching of the active layer of the structure, stopping the etching depth at the buried oxide insulating layer (remember that examples discussed in this description relate to an SOI),

➤ Solid plate metallic deposit on the structure, above the buried oxide with an electrically conducting metal. A one-micron thickness of aluminium can thus be deposited,

5 ➤ Dry and selective etching of the deposited metal to form test patterns, actually parallel conducting metallised lines (that form wave guides);

• Application of an electrical signal on one of the metallised lines. This signal V_A consists of a
10 superposition of a DC voltage V_{DC} and a low amplitude AC voltage V_{AC} . It is applied to the said line, and the following can be modified:

➤ the amplitude of the DC component V_{DC} ,

➤ the frequency of the AC component V_{AC} ,

15 • Calculation of losses (α = losses in conductors α_{COND} + losses in the layers located below the active layer before it is eliminated by etching α_{SUB}), making use of measurements of emitted, transmitted and reflected powers at the ends of the wave guide.

20 ➤ α_{SUB} is extracted from values of α and an estimate of α_{COND} that is considered as being fixed for a given frequency of the applied signal.

The principle of this method is illustrated in Figure 3, that in particular illustrates the wave guides
25 created in different regions of a structure for which losses are to be characterised (the voltage V_A is applied to the central conductor of each coplanar line).

The advantage of superposing a DC component on the AC component during the measurements is to demonstrate the

considerable effect on losses of a layer with low resistance under the insulation / support layer interface in structures concerned by the invention.

As will be explained in more detail in the remainder of this text, this low resistance layer is generated by application of the DC component under the central conductor of the wave guides.

It is also strongly influenced by the parameters Q_{BOX} and D_{it} . Therefore, the concentration of carriers in this low resistance layer and its global volume (controlled in particular by its thickness), is the reason why Q_{BOX} and D_{it} have an effect on the losses.

Losses measured during implementation of this method are used to extract an effective resistivity of the structure (this effective resistivity being directly related to losses).

As mentioned above, and as will be illustrated in detail, the applicants use the demonstrated influence of the following:

- the charge of (i.e. within) the buried oxide insulating layer Q_{BOX} ,
- the density of carrier traps D_{it} ,

on structure losses, within the context of the invention.

Simulations, for which the results are illustrated in Figures 1 and 2, thus demonstrate the corresponding influence of the parameters Q_{BOX} (Figure 1) and D_{it} (Figure 2) on losses associated with a structure concerned by the invention.

The curves of these two figures are derived from a simulation model that calculates the parallel linear conductance (G_{EFF}) of coplanar wave guides made on a structure.

5 Figure 3 shows coplanar wave guides made on a structure, and an equivalent distributed circuit (in the right part of the figure).

The propagation exponent γ associated with the coplanar wave guide is in the form: $\gamma = (\alpha_{cond} + \alpha_{sub}) + j\beta =$
 10 $\sqrt{(Reff + j\omega Leff) \cdot (Geff + j\omega Ceff)}$

The losses α_{SUB} associated with the support layer in the structures are directly proportional to G_{EFF} at high frequencies.

Losses α_{SUB} are equal to $[0.5 * G_{EFF} (L_{eff} / C_{eff})^{0.5}]$, where L_{eff}
 15 and C_{eff} denote the linear inductance and capacitance respectively of the coplanar structure shown in Figure 3.

For a given structure, the losses associated with the structure therefore increase with the value of the parameter G_{EFF} (and vice versa).

20 The model used is implemented by the Atlas software (registered trademark) of the Silvaco Company. This model is active for taking account of the different dimensional parameters of the coplanar wave guide:

- geometry of metallised lines formed on the
 25 structure for measurement of losses,
- thickness of the buried oxide layer (insulating layer) of the structure,

• voltage V_A applied on the metallised lines (polarisation voltage and frequency taken into account).

Furthermore, this model takes account of the parameters D_{it} and Q_{BOX} in the calculation of G_{EFF} .

5 Figure 1 shows 4 curves 11, 12, 13 and 14 corresponding to four different structures associated with four different values of the parameter Q_{BOX} .

Each of these curves illustrates the relative variation of structure losses with respect to a reference
10 point (through the parameter G_{EFF} that is directly related to losses as described above), as a function of a voltage V_A that will be applied to a conductor of the structure in the context of the loss measurement method described above.

The reference point is fixed to the value of G_{EFF}
15 obtained for $V_{DC} = Q_{BOX} = D_{it} = 0$.

Curve 11 corresponds to a structure for which the value Q_{BOX} is zero.

Curves 12, 13 and 14 correspond to three structures for which the insulating layers have non-zero values of
20 Q_{BOX} , increasing from the structure of the curve 12 to the structure of the curve 14 (for which the charge of the insulating layer is equal to 10^{11} cm^{-2}).

The arrow in this figure shows an increase of Q_{BOX} between the structures in the different curves.

25 This figure illustrates that an increase in the value of Q_{BOX} causes an increase in structure losses.

This influence of the parameter Q_{BOX} , and therefore the charge of the electrically insulating layer, can be explained as follows.

This charge is a positive charge, which therefore tends to attract mobile negative charges (electrons) to the interface between the insulating layer and the support layer (very resistive).

- 5 An excess of these electrons collects at the said interface then forming a surface layer with low resistance, that therefore increases global losses in the support layer.

10 During implementation of the loss measurement method mentioned above, a slightly negative voltage V_A can be applied to the central conductor to only temporarily push these electrons under the central conductor, which then move away from the interface; this part of the interface then becomes more resistive and the measured losses are
15 reduced.

If now the value of V_A is further reduced, the positive mobile charges will in turn be attracted towards the interface and thus locally reduce its resistivity.

The loss is thus minimum for a negative voltage V_{OPT} .
20 This shift in the minimum losses is illustrated in Figure 1.

Thus, as the value of Q_{BOX} increases, the value of V_{OPT} shifts towards negative values.

25 Similarly, for a large value of Q_{BOX} , the presence of electrons at the interface between the buried oxide insulating layer and the support layer will increase losses (even at V_{OPT} which is the voltage at which the electrons attracted to the insulation / support layer as described above are not present under the central conductor to which

the voltage V_A is applied, but are present at other locations of the interface).

Therefore, an increase in the value Q_{BOX} between two identical structures induces an increase in losses and a shift towards negative potentials of the value V_{OPT} of V_A for which losses are minimum, as can be seen in figure 1.

Similarly, Figure 2 shows three curves 21, 22, 23 corresponding to three different structures.

Each structure is associated with a different value of D_{it} , at the interface between its electrically insulating layer and its support layer.

Each of these three curves has a minimum near the zero volt abscissa (therefore corresponding to almost identical values V_{OPT}).

Curve 21 corresponds to a structure associated with a zero value of D_{it} .

Curves 22 to 24 correspond to structures with a non-zero and increasing D_{it} (from curve 22 to curve 24), the D_{it} associated with the structure of the curve 24 being 10^{12} $\#/\text{cm}^2/\text{eV}$.

The two arrows on each side of the minimum of the three curves represent this increase in D_{it} between the three structures.

It can be seen that an increase in D_{it} reduces losses associated with the structure.

It can also be seen that an increase in D_{it} reduces the influence of the DC component of the constant voltage V_{DC} applied to the central metallised line of the structure.

This influence of the parameter D_{it} on losses can be explained as follows:

This parameter characterises the density of traps such as sharp edges, contaminants, or any other trap that could trap a positive or negative mobile charge (electron or hole - which is a vacant space in the crystalline lattice of the material) at the interface between the insulation and the support layer of the structure.

A high density at this interface will tend to counter the influence mentioned above related to the tendency to increase the charge of the insulating layer.

A high density causes absorption of some electrons that arrive and form the surface layer at the said interface and which has the effect of reducing the resistivity (and therefore increasing the losses) of the structure.

This effect increases (therefore tending to reduce losses) as the density increases.

Furthermore, the effect of the voltage V_A that attracts electrons or positive charges to the said interface (depending on the sign of this voltage) is attenuated by a higher carrier traps density; in this case, some mobile charges attracted towards the interface by the voltage V_A are trapped, and thus neutralised so that they have no influence on losses.

Note that the increase in the density of carrier traps is thus applicable in the same way for positive or negative voltages V_A .

The graph in figure 4 illustrates the effect of a variation of the parameter D_{it} on losses α .

This graph contains two curves, corresponding to two different structures:

- An SOI structure obtained by the applicants without any particular treatment (following a SMARTCUT® process), (shown in solid lines, curve 41).

- A similar structure subjected to a specific treatment aimed at reducing the value of the parameter D_{it} at the interface between the buried oxide insulating layer and the support layer of the structure (dashed line, curve 42). This treatment may be annealing under a mix composed of 5% hydrogen and 95% nitrogen, at a temperature of the order of 432°C for 30 minutes.

In the remainder of the text, we will come back to the special treatment used to obtain this reduction of the parameter D_{it} .

Figure 4 thus illustrates that a reduction of D_{it} at the interface between the insulating layer and the support layer of the structure increases losses through the structure.

Correspondingly, Figure 5 illustrates the influence of a modification of the value of Q_{BOX} on losses α .

Figure 5 thus represents the variation of losses as a function of the constant voltage applied during characterisation of these losses, for two different structures:

- A structure with a low Q_{BOX} , for example of the order of $1.5 \times 10^{10} \text{ cm}^{-2}$ (curve 51 that corresponds to an SOI obtained in a manner known in itself by a SMARTCUT® process);

- And a structure with a higher Q_{BOX} , of the order of $6 \times 10^{10} \text{ cm}^{-2}$ (curve 52 that corresponds to an oxidised

High Resistivity Si wafer in a furnace containing a contaminant - for example a metallic contaminant).

Note that an increase in the parameter Q_{BOX} will increase losses, as already mentioned above.

- 5 Note that the level of D_{it} has not been modified between structures corresponding to curves 51 and 52 respectively.

10 The curves in figure 7 show the variation of losses for $V_{DC} = 0$ V as a function of the frequency, for three SOI structures obtained by a SMARTCUT® process with different values of Q_{BOX} and D_{it} .

The following table gives values of Q_{BOX} and D_{it} for each of these three structures SL1, SL2, SH1.

Wafer name	Q_{BOX} [$\#/cm^2$]	D_{it} [$\#/cm^2/eV$]
SL1	$\sim 1^{e10}$	Negligible
SL2	$\sim 1^{e10}$	$\sim 1^{e11}$
SH1	$\sim 1^{e10}$ where $Q_{BOX.SH1} > Q_{BOX.SL1}$	Negligible

15

The curves in dashed lines correspond to simulated losses of coplanar wave guides made on identical structures, except for the resistivity ρ_{eff} of the support layers of these corresponding structures that vary from 100 $\Omega.cm$ (top curve) to 5000 $\Omega.cm$ (bottom curve - resistivity values of the support layers increase in the direction of the arrow).

20

The figure shows that theoretical losses reduce as this resistivity ρ_{eff} increases.

Note that these theoretical losses contain losses associated with metallic conductors of lines (corresponding to the lowest curve in figure 7, shown in continuous lines) and losses in the support layer.

5 Figure 7 shows that the structure with the highest value of D_{it} is the structure that has the lowest losses. Losses in this structure correspond to an effective resistivity of the order of 4000 $\Omega\cdot\text{cm}$, which makes losses associated with the support layer negligible compared with
10 losses associated with metallic conductors (since total losses α are equal to the sum of losses α_{COND} and α_{SUB} when α_{SUB} tends towards zero, α becomes equivalent to α_{COND}).

Structures with low values of Q_{BOX} but negligible values of D_{it} have losses corresponding to resistivity
15 values of the support layer equal to 300 and 500 $\Omega\cdot\text{cm}$ only.

In the case of the invention, a value of the density of carrier traps and / or a value of charges within the electrically insulating layer of a structure concerned by the invention are thus modified, in order to maximise the
20 electrical resistivity of this structure.

And as will be further explained in this text, the density of carrier traps is modified at the interface between a buried layer (e.g. buried oxide of a SOI) and the underlying support layer.

25 As mentioned above, the invention may be implemented in the context of bonding a first substrate (comprising the active layer of the structure), and a second substrate (comprising the structure support layer).

In this case, the first substrate that includes the active layer of the structure may also include the insulating layer of the structure.

Before performing this type of bonding, it is possible
5 to modify the density of the carrier traps to increase this density, which as seen above will reduce losses associated with the structure.

Consequently, several variants may be envisaged (either implemented alone or in combination):

10 • Modification of the density of carrier traps by inserting an intermediate layer between the two substrates to be bonded, designed to come into contact with the support layer of the second substrate, the material of the said intermediate layer being chosen so as to facilitate an
15 increase in the density of carrier traps, due to its association with the material from which the support layer is made;

> In this case, the said intermediate layer can be deposited on the second substrate, prior to bonding;

20 > And in one application of the invention, the support layer may be made of silicon and the intermediate layer material may be a nitrided oxide;

• Modification of the density of carrier traps, using at least one material for bonding the said first and
25 second substrates, that facilitates an increase in the density of carrier traps as a result of its association with the material from which the support layer is made;

• Modification of the density of the carrier traps by applying a treatment in the surface region of the second

substrate, before the said first and second substrates are bonded;

> This type of treatment of the surface region of the second substrate may in particular include a controlled
5 deterioration of the surface condition of this second substrate (deterioration of its roughness by etching).

In all variants presented above, the density of carrier traps is modified in the resulting structure at the interface between the oxide layer and the underlying
10 support layer.

Moreover, still within the context of the invention when used in combination with bonding like that mentioned above, the charge within the electrically insulating layer of the structure can be modified so as to reduce it,
15 according to different variants (once again applied alone or in combination):

- Modification of the charge by adjusting the characteristics of an implantation made in the said first substrate before bonding;

20 > In this case, the doses of the implantation are preferably adjusted to modify the charge value in the electrically insulating layer;

> This implantation may also correspond to the step in which a weakening implantation is made using a SMARTCUT®
25 type process. In this case, the first substrate may be a monocrystalline silicon substrate with a surface that is oxidised before implantation takes place through this oxidised surface, and the second substrate corresponds to the support or stiffener that will be bonded to the said
30 first substrate - this first substrate then being separated

at the weakening area with a thickness defined in the implantation step, to result in the desired multilayer structure.

- Modification of the charge in the electrically insulating layer by adjusting the parameters of a thermal oxidation made on the first substrate before bonding, to create the insulating layer of the structure at its surface;

- > The parameters on which action is taken include particularly the temperature (absolute value) and / or its variation (particularly the characteristics of the temperature rise gradient), the gas composition and the annealing time;

- > Once again, the said thermal oxidation may correspond to the step in which an oxide layer is created using a SMARTCUT ® type process.

Finally, it is also possible to modify the charge within the electrically insulating layer of the structure by adjusting the parameters of a heat treatment that is applied to the said structure once it has been formed. In this case, it is indifferent whether or not the two substrates have been bonded beforehand.

And in this type of variant adjustment of the charge in the electrically insulating layer of the structure, the thermal budget of the said heat treatment is adjusted so as to minimise the charge in this insulating layer.

It is to be noted that modifying the charge within the electrically insulating layer of the structure is quite distinct from influencing the repartition of charges at

some interfaces between layers of a structure (the latter technique being disclosed e.g. by US 6 091 112).

Furthermore, regarding US 6 091 112, this document does in any event not aim at minimizing the losses in the support layer - as the invention does - but it rather aims at avoiding depletion in the active layer. In this respect, this prior art document proposes to influence the characteristics of the active layer, but not of a buried insulating layer (as it is the case for the invention).

Figure 6 shows the bonding step for two substrates A and B mentioned above, in the case in which the substrate A has been oxidised (in particular to create a surface oxide layer A1) and an implantation (to create a weakening area A2 defining an active layer A3 within the thickness of substrate A).

The substrate B corresponds to the support layer of the required final structure.

This case corresponds particularly to the use of the invention in the context of a SMARTCUT® type process.

CLAIMS

1. Process for manufacturing a multilayer structure made from semiconducting materials and comprising an active layer, a support layer and an electrically insulating layer between the active layer and the support layer,
5 characterised in that the process comprises modification of the density of carrier traps and / or the electrical charge within the electrically insulating layer, in order to minimise electrical losses in the structure support layer.

2. Process according to the previous claim,
10 characterised in that the said modification aims at increasing the density of carrier traps at the interface between the structure insulating layer and the underlying structure support layer.

3. Process according to one of the previous claims,
15 characterised in that the said modification aims at reducing the electrical charge in the electrically insulating layer of the structure.

4. Process according to one of the previous claims, characterised in that the active layer is selected so as to
20 have a resistivity significantly lower than the resistivity of the support layer.

5. Process according to one of the previous claims, characterised in that the process includes bonding of a first substrate comprising the structure active layer and a
25 second substrate comprising the structure support layer.

6. Process according to the previous claim, characterised in that the said first substrate comprises an insulating layer.

7. Process according to the previous claim, characterised in that the said insulating layer of the first substrate corresponds to the insulating layer of the structure.

5 8. Process according to one of the three previous claims, characterised in that in order to minimise electrical losses in the structure support layer, the density of the carrier traps is modified before the said first substrate and the said second substrate are bonded.

10 9. Process according to the previous claim, characterised in that in order to minimise electrical losses in the structure support layer, the density of the carrier traps is modified by inserting an intermediate layer between the said two substrates to be bonded, that
15 will come into contact with the support layer of the second substrate, the material of the said intermediate layer being chosen so as to increase the density of the carrier traps, due to its association with the material in the said support layer.

20 10. Process according to the previous claim, characterised in that the said intermediate layer is deposited on the said second substrate, before the said bonding of the first and second substrates.

25 11. Process according to the previous claim, characterised in that the said support layer is made of silicon and the material used in the said intermediate layer is a nitrided oxide.

30 12. Process according to one of the four previous claims, characterised in that the density of carrier traps is modified using at least one material that tends to

increase the density of carrier traps due to its association with the material in the said support layer, for bonding the said first and second substrates, to minimise electrical losses in the structure support layer.

5 13. Process according to one of the five previous claims, characterised in that the density of carrier traps is modified by applying a treatment to the surface region of the second substrate before the said first and second substrates are bonded, in order to minimise electrical
10 losses in the structure support layer.

14. Process according to the previous claim, characterised in that the said treatment of the surface region of the second substrate includes controlled deterioration of the surface condition of the second
15 substrate.

15. Process according to one of the seven previous claims, characterised in that in order to minimise electrical losses in the structure support layer, the charge is modified within the electrically insulating layer
20 by adjusting the characteristics of an implantation made in the said first substrate before the said first and second substrates are bonded.

16. Process according to the previous claim, characterised in that the doses of the said implantation
25 are adjusted to modify the charge in the electrically insulating layer.

17. Process according to one of the two previous claims, characterised in that the said implantation corresponds to a weakening implantation of a SMARTCUT® type
30 process.

18. Process according to one of the ten previous claims, characterised in that in order to minimize electrical losses in the structure support layer, the charge within the electrically insulating layer is modified
5 by adjusting the parameters of a thermal oxidation made on the said first substrate to create the structure insulating layer on its surface.

19. Process according to the previous claim, characterised in that the said parameters include the
10 temperature and / or temperature variation, the gas composition, annealing times.

20. Process according to one of the previous claims, characterised in that the charge within the electrically insulating layer is modified by adjusting the parameters of
15 a heat treatment that is applied to the said structure once the structure has been formed, in order to minimise electrical losses in the structure support layer.

21. Process according to the previous claim, characterised in that the thermal budget of the said heat
20 treatment is adjusted so as to reduce the charge in the electrically insulating layer of the structure.

22. Process according to one of the previous claims, characterised in that the said structure is an SOI.

23. Process according to one of the previous claims,
25 characterised in that the process uses the steps in a SMARTCUT® type process.