Claims

What is claimed:

1. A semiconductor device, comprising:

a semiconductor die;

a stress relief buffer including a compliant material for absorbing thermo-mechanical stress disposed partially around the semiconductor die and away from the semiconductor die in ~~a~~ separate locations designated for bump formation;

an encapsulant deposited between the stress relief buffer and semiconductor die; and between the separate locations of the stress relief buffer with the stress relief buffer extending through a thickness of the encapsulant; and

an interconnect structure formed over the semiconductor die and stress relief buffer, the interconnect structure including a plurality of bumps formed over the stress relief buffer and coupled ~~electrically connected~~ to the semiconductor die.

2. The semiconductor device of claim 1, wherein the stress relief buffer includes a multi-layer composite material.

3. The semiconductor device of claim 1, wherein the stress relief buffer includes:

~~forming~~ a first compliant layer;

~~forming~~ a silicon layer formed over the first compliant layer; and

~~forming~~ a second compliant layer formed over the silicon layer.

~~4. The semiconductor device of claim 1, further including a stiffener layer formed over the stress relief buffer and encapsulant.~~

~~5~~4. The semiconductor device of claim 1, wherein the stress relief buffer is disposed along a side or at a corner of the semiconductor die.

~~6~~5. The semiconductor device of claim 1, wherein the stress relief buffer is further disposed around ~~at a corner of~~ the semiconductor die and continuous from a first side of the semiconductor die to a second side of the semiconductor die opposite the first side.

~~7~~6. A semiconductor device, comprising:

a semiconductor die or component;

a compliant stress relief buffer for absorbing thermo-mechanical stress disposed in separate ~~at~~ locations around the semiconductor die or component;

an encapsulant deposited around the semiconductor die or component; and between the separate locations of the compliant stress relief buffer; and

an interconnect structure formed over the semiconductor die or component and ~~stress relief buffer, the interconnect structure being electrically connected to the semiconductor die or component~~ a first surface of the compliant stress relief buffer with a second surface of the compliant stress relief buffer being devoid of the encapsulant.

~~8~~7. The semiconductor device of claim ~~7~~6, wherein the compliant stress relief buffer includes a multi-layer composite material.

~~9~~8. The semiconductor device of claim ~~7~~6, wherein the compliant stress relief buffer includes:

~~forming~~ a first compliant layer;

~~forming~~ a silicon layer formed over the first compliant layer; and

~~forming~~ a second compliant layer formed over the silicon layer.

~~10~~9. The semiconductor device of claim ~~7~~6, further including a stiffener layer formed over the compliant stress relief buffer and encapsulant.

1~~1~~0. ~~The semiconductor device of claim 7, further~~ A semiconductor device, comprising:

a semiconductor die or component;

a stress relief buffer disposed at locations around the semiconductor die or component including a circuit layer formed within the stress relief buffer;

an encapsulant deposited around the semiconductor die or component; and

an interconnect structure formed over the semiconductor die or component and stress relief buffer, the interconnect structure being electrically connected to the semiconductor die or component. ~~including a circuit layer formed within the stress relief buffer.~~

121. The semiconductor device of claim 710, wherein the encapsulant is further disposed over the stress relief buffer.

132. The semiconductor device of claim 710, further including a plurality of bumps formed over the stress relief buffer.

143. A semiconductor device, comprising:

a semiconductor die or component;

a stress relief buffer including a compliant material for absorbing thermo-mechanical stress disposed around ~~outside a footprint of~~ the semiconductor die or component including a singulated portion of the stress relief buffer; and~~;~~

an encapsulant deposited around the semiconductor die or component~~; and~~

~~an interconnect structure formed over the semiconductor die or component~~ and stress relief buffer.

154. The semiconductor device of claim 143, wherein the stress relief buffer includes a multi-layer composite material.

165. The semiconductor device of claim 143, further including a stiffener layer formed over the stress relief buffer~~ and encapsulant~~.

176. The semiconductor device of claim 143, wherein the stress relief buffer is disposed along a side or at a corner of the semiconductor die or component.

187. The semiconductor device of claim 143, wherein the encapsulant is disposed over the stress relief buffer.

198. The semiconductor device of claim 143, further including a plurality of bumps formed over the stress relief buffer.

19. The semiconductor device of claim 13, wherein the stress relief buffer is disposed in separate locations around the semiconductor die or component.

20. The semiconductor device of claim 19, wherein the encapsulant is deposited between the separate locations of the stress relief buffer.

21. The semiconductor device of claim 13, further including an interconnect structure formed over the semiconductor die and stress relief buffer.

2~~0~~2. A semiconductor device, comprising:

a semiconductor die or component;

a stress relief buffer including a compliant material for absorbing thermo-mechanical stress disposed around the semiconductor die or component; and

an encapsulant deposited around the semiconductor die or component and stress relief buffer.

2~~1~~3. The semiconductor device of claim 2~~0~~2, further including an interconnect structure formed over the semiconductor die or component and stress relief buffer, the interconnect structure being electrically connected to the semiconductor die or component.

2~~2~~4. The semiconductor device of claim 2~~0~~2, wherein the stress relief buffer includes a multi-layer composite material.

2~~3~~5. The semiconductor device of claim 2~~0~~2, wherein the stress relief buffer is disposed along a side or at a corner of the semiconductor die or component.

2~~4~~6. The semiconductor device of claim 2~~0~~2, further including a stiffener layer formed over the stress relief buffer and encapsulant.

~~25. The semiconductor device of claim 20, wherein the encapsulant is disposed over the stress relief buffer.~~

27. The semiconductor device of claim 22, wherein the stress relief buffer is disposed in separate locations around the semiconductor die or component.

28. The semiconductor device of claim 27, wherein the encapsulant is deposited between the separate locations of the stress relief buffer.