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TRENCH DEPLETION MOSFET

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to high power MOSFET transistors and, more particularly, to high power MOSFET transistors with low on-resistance employing a trench MOS gate structure.

2. Description of the Related Art:

To optimize the power-handling capability of any power semiconductor device, it is essential to maximize the cell packing density. It has become evident both experimentally and analytically that device physics limitations are restricting further advances in cell packing density, and thus in MOSFET performance, using a surface channel formed by the self-aligned double-diffused process, commonly known as DMOS.

An improvement in cell packing density can be achieved by utilizing a trench MOS gate structure rather than a standard DMOS structure. The lack of JFET pinching effect in a trench gate structure also results in a significantly lower on-state resistance compared with a DMOS structure. Low on-resistance is particularly important when MOSFETs are used in low-frequency power electronic applications, such as automotive electronics.

A conventional trench power MOSFET is shown in Fig. 1. The device includes an N^+ source region 2, a P base or channel region 4, an N^- region 6 and an N^+

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region 8. A polysilicon gate 10 is formed in trenches on both sides of P base 4 and separated therefrom by a thin layer of oxide 11. A source electrode 12 on the upper surface of the device covers source region 2. A drain electrode 14 on the bottom surface of the device covers N^+ region 8.

The operation of the device of Fig. 1 is as follows. With the drain electrode 14 positive with respect to the source electrode 12, current flows upward through the device when a positive potential is applied to gate 10. The positive potential on gate 10 inverts P base 4, forming an n-channel therethrough, permitting current to flow from drain to source.

While the trench power MOSFET of Fig. 1 has significant advantages over a DMOS transistor in terms of cell packing density, the inclusion of a P base in the structure undesirably contributes to on-resistance, because of channel resistance when the p-channel is inverted. This sets a limit on the amount that on-resistance can be reduced in a DMOS device. Additionally, the conventional trench power MOSFET shown in Fig. 1 has a parasitic P-N junction, which presents a problem during synchronous rectification.

An enhancement type of structure for a trench power MOSFET is shown in Fig. 2, wherein like elements are indicated by like reference numerals. This device, described by B. Baliga, "The Accumulation-Mode Field-Effect Transistor: A New Ultralow On-Resistance MOSFET," IEEE Electron Device Letters, Vol. 13, No. 8, August 1992, pp. 427-29), does not contain a P base region, and therefore has no P-N junction between the source and

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drain regions. Unlike the depletion type trench power MOSFET shown in Fig. 1, current conduction in the device of Fig. 2 occurs along the surface of an accumulation layer formed along the trench sidewalls, resulting in a much lower on-resistance. Additionally, in the device of Fig. 2, a drift region doping below $1x10^{14}$ cm^{-3} can be used, while an optimal drift region doping of $2x10^{16}$ cm^{-3} is required for the trench power MOSFET of Fig. 1. Further, the structure of Fig. 2 advantageously does not contain a parasitic P-N junction.

In order to turn off the device of Fig. 2, a potential is applied to gate 10 to invert the N^- region 6. However, in the Fig. 2 device, the depletion width due to the MOS gate is limited by the formation of an inversion layer of holes in the N^- drift region. This limits the forward blocking capability of the device.

SUMMARY OF THE INVENTION

The present invention is a trench power MOSFET with a unique structure which overcomes the above-noted deficiencies of the prior art.

Advantageously, the present invention, like the trench power MOSFET of Fig. 2, does not have a P base region and thus has no P-N junction. Thus, the trench power MOSFET of the present invention is formed in a wafer of semiconductor material having first and second (i.e. upper and lower) opposing semiconductor surfaces, the wafer of semiconductor material including a relatively lightly doped region of a first conductivity type, preferably N^-, a plurality of spaced narrow

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trenches perpendicularly formed in the wafer and extending from the upper surface of the wafer, at least a portion of the N^- region being disposed between the trenches from the upper semiconductor surface. Polysilicon gates are disposed in the trenches and spaced from the intervening portion of the N^- region by a layer of gate insulation material. A first relatively highly doped region of the first conductivity type, i.e. N^+, is disposed between and adjacent to the upper semiconductor surface and the N^- region.

The present invention is an improvement over the prior art device of Fig. 2, however, by the inclusion, in a first embodiment, of a P^+ region formed in the wafer and extending from the upper surface of the wafer at a position adjacent to and at least partially co-extensive with the upper N^+ region, i.e. the source region. On application of a negative gate voltage to turn the device off, the added P^+ region forms a drain for holes generated in the N^- region. Thus, as soon as the holes are formed, they are swept off towards the P^+ region by the electric field, via a trench p-channel MOSFET . This effect is hereinafter termed "deep-depletion."

The deep-depletion very efficiently pinches off the N^- region between the trench MOS gates, forming a potential barrier to the flow of electrons and greatly improving the forward blocking capability of the device. Unlike the prior art structure of Fig. 2, the depletion width due to the MOS gate is not limited by the formation of an inversion layer of holes. This allows the trench

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gates in the structure of the present invention to be spaced farther apart, improves breakdown voltage, reduces leakage current and simplifies fabrication.

In the on-state, with a positive voltage on the gate, the current conduction, as in the prior art Fig. 2 device, is mainly through an accumulation layer formed on the silicon surface on the side of the trench. Since the effective mobility of the electrons in the accumulation region is higher than that through the inversion region, the on-resistance of the device of the present invention, like the prior art device of Fig. 2, is still lower than the conventional trench power MOSFET.

In a second embodiment of the invention, a P^+ diffusion is formed centrally within the N^+ region between the gates. The P^+ diffusion causes pinch-off of the portion of the N^- region between the P^+ diffusion and the MOS gate (i.e. a JFET action) with a negative potential applied to the gate.

In yet another embodiment of the invention, a P^+ region is formed both at the upper surface of the device, spaced from the N^+ source (as in the first embodiment), and formed centrally within the N^+ region between the gates (as in the second embodiment of the invention).

The present invention further preferably includes an N^+ region between and adjacent to the lower semiconductor surface and the N^- region (in a MOSFET embodiment) or a P^+ region between and adjacent to the lower semiconductor surface of the device and the N^- region, thereby forming a structure consisting of a PN

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diode in series with a trench MOSFET (i.e. an IGBT embodiment).

Advantageously, all embodiments of the invention can be implemented in a cellular geometry with ring shaped trenches spaced from one another over the surface of the silicon. Additionally, in all embodiments, the overlap between the N^- region and the gate can be varied to optimize either breakdown voltage or on-resistance performance of the device.

The present invention may also be provided in a horizontal conduction configuration, in which case the gate is disposed on the upper surface of the device over the N^- drift region, rather than in trenches.

Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows the configuration of a prior art depletion type trench power MOSFET.

Fig. 2 shows the configuration of a prior art enhancement type trench power MOSFET.

Fig. 3 shows a first embodiment of the present invention with an added P^+ drain region extending from the upper surface of the enhancement type device; Fig. 3a shows a cross-section of multiple cells of the first embodiment of the present invention; Fig. 3b shows a top view of multiple cells of the first embodiment of the present invention.

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Fig. 4 shows a second embodiment of the present invention with a P^+ region diffused from the upper surface of the wafer centrally through the N^+ source region and into the N^- drift region between the trench gates.

Fig. 5 shows a combined embodiment of the invention provided with the P^+ regions of both Fig. 3 and Fig. 4; Fig. 5a shows an alternative configuration of Fig. 5 with the central P^+ region extending all the way to the N^+ drain region.

Figs. 6 and 7 show an alternative configuration corresponding to the embodiments of Figs. 3 and 4, respectively, which has a shallower N^- drift region and thus a lower on-resistance, but also a lower breakdown voltage.

Figs. 8 and 9 show another alternative configuration corresponding again to the embodiments of Figs. 3 and 4, respectively, with an even shallower N^- drift region than the embodiment of Figs. 6 and 7.

Figs. 10, 11 and 12 show a top view of a preferred hexagonal cell configuration for the embodiments of Figs. 3, 4 and 5, respectively.

Figs. 13-15 show yet an IGBT embodiment of the invention in which the N^+ region at the lower surface of the device is replaced by a P^+ region.

Fig. 16 shows a horizontal conduction embodiment of the invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A first embodiment of the novel trench power MOSFET of the present invention is shown in Fig. 3. As shown therein, the present invention has a structure similar to the prior art device of Fig. 2, but additionally includes a P^+ region 16 formed in the wafer and extending from the upper surface of the wafer (covered by source electrode 12) adjacent to N^+ source region 2.

As shown by the arrow in Fig. 3, when the device is in the off (forward blocking state), with a negative potential applied to gate 10, P^+ region 16 advantageously sweeps off holes formed in N^- region 6 via a trench p-channel MOSFET in which P^+ region 16 acts as the "drain", gate electrode 10 is the "gate", N^- region 6 is the "channel" (inverted by the gate) and the holes formed by the inversion of N^- region 6 are the "source". P^+ region 16 thus acts as a drain for the holes, resulting in the following advantages:

First, P^+ drain region 16 prevents the formation of an inversion layer of holes when the device is in the off-state and thus overcomes a primary limitation on the performance of the prior art Fig. 2 device, namely a limitation on the depletion depth adjacent the gate. Thus, P^+ drain region 16 of the present invention causes increased depletion ("deep-depletion") adjacent the gate in the off-state. This increases the potential barrier for the flow of electrons between source 12 and drain 14 in the off-state, which

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leads to reduced leakage current and higher breakdown voltage.

Second, the elimination of an inversion layer of holes in the present invention eliminates band-to-band tunneling leakage current, which is a significant leakage mechanism in VLSI devices, including the Fig. 2 device.

The embodiment of the present invention shown in Fig. 3 was simulated with the parameters shown in the following Table:

PARAMETER	VALUE
Cell pitch (see Fig. 3b)	3 μm
N- drift region doping	$1x10^{14}$ cm^{-3}
Trench depth	4 μm
Trench width	2 μm
Distance between trenches (see Fig. 3b)	1 μm
Gate oxide thickness	500 Å
Source metal contact window	0.8 μm
P+ surface concentration	$1x10^{20}$ cm^{-3}
P+ junction depth	0.3 μm
N+ source surface concentration	$1x10^{18}$ cm^{-3}
N+ source junction depth	0.7 μm

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The results of the simulation using the foregoing parameters showed a forward blocking voltage in excess of 60 V. The on-resistance R_{ON} was found to be 0.076 $m\Omega$-cm^2, which is significantly lower than the on-resistance of conventional trench power MOSFETs. Fully gate controlled characteristics and a threshold voltage of 0.8 V was obtained. Theoretical calculations of R_{ON} using the various components of on-resistance agree closely with these results.

Referring now to Fig. 4, a second embodiment of the present invention is shown in which a P^+ region 18 is diffused from the upper surface of the wafer centrally through N^+ source region 2 and into N^- drift region 6. Forward blocking in this embodiment is achieved by depletion from MOS gate 10 and a junction depletion (JFET action) from P^+ diffusion 18.

Optionally, as shown in Fig. 5, the present invention can be provided in an embodiment with both P^+ drain region 16 and P^+ diffusion 18, and with the accompanying advantages of each. Fig. 5a shows an alternative configuration of Fig. 5 with the central P^+ region 18 extending all the way down to the N^+ region 8.

Figs. 6 and 7 show an alternative configuration corresponding to the embodiments of Figs. 3 and 4, respectively, which has a shallower N^- drift region 6 and thus a lower on-resistance, but also a lower breakdown voltage. Figs. 8 and 9 show another alternative configuration again corresponding to the embodiments of Figs. 3 and 4, respectively, with an even shallower N^- drift region 6 than the embodiment of Figs. 6 and 7. The

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embodiment of Figs. 8 and 9 has the lowest on-resistance, but can only be used in low voltage applications due to its relatively low breakdown voltage.

Advantageously, the present invention can be provided in a cellular topology. For example, Figs. 3a and 3b show a cross-section and top view, respectively, of multiple cells of the embodiment of Fig. 3. Alternatively and preferably, each of the unit cells can be provided in a polygonal configuration. Figs. 10, 11 and 12 show the top view of a preferred hexagonal cell configuration for the embodiments of Figs. 3, 4 and 5, respectively.

Figs. 13-15 show yet another embodiment of the invention in which N^+ region 8 is replaced by a P^+ region 20. Thus, as shown in Fig. 13, the prior art Fig. 2 structure can be modified to form a PN junction in series with a trench transistor, thereby creating an IGBT device. Likewise, Figs. 14 and 15 show the IGBT configuration corresponding to the embodiments of Figs. 3 and 4, respectively.

Although not shown, the combined embodiment of the invention shown in Fig. 5 can be similarly provided in an IGBT configuration. Likewise, the IGBT configurations can be implemented in a cellular topology (corresponding to Figs. 10-12) and/or with the shallower N^- drift regions 6 shown in Figs. 6-9 to improve on-resistance in lower voltage applications.

Fig. 16 shows a horizontal conduction embodiment of the invention in which the device is formed on a P^+ substrate 22. In the on-state, current flows

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from N^+ drain region 24, through N^- drift region 26 to N^+ source region 28. As in the corresponding vertical conduction embodiment of Fig. 3, a P^+ drain region 30 is formed in the semiconductor wafer and extends into the wafer from the upper surface thereof at a position adjacent to the N^+ source region 28. A MOS gate 32 overlies N^- drift region 26.

On application of a negative voltage to MOS gate 32, P^+ region 30 forms a drain for holes generated in N^- drift region 26. Thus, again, as soon as the holes are formed, they are swept off towards P^+ region 30 by the electric field, via a lateral p-channel MOSFET, resulting in "deep-depletion" of N^- drift region 26.

Obviously, many other variations of the present invention are possible. For example, in all of the previously described embodiments, the doping polarities of the regions and applied voltages could be reversed, such that current would flow in the opposite direction.

Thus, although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

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WHAT IS CLAIMED IS:

1. A high power metal oxide semiconductor field effect trench transistor device exhibiting relatively low on-resistance and relatively high breakdown voltage, said device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces, said wafer of semiconductor material including a relatively lightly doped region of a first conductivity type, a plurality of spaced narrow trenches perpendicularly formed in said wafer and extending from said first semiconductor surface, at least a portion of said relatively lightly doped region being disposed between said trenches;

gate electrode means disposed in said trenches and spaced from said portion of said relatively lightly doped region by a layer of gate insulation material;

a first relatively highly doped region of said first conductivity type disposed between and adjacent to said first semiconductor surface and said relatively lightly doped region; and

a first region of a second conductivity type opposite to said first conductivity type, said first region of said second conductivity type being formed in said wafer and extending from said first semiconductor surface adjacent to said first relatively highly doped region of said first conductivity type, said first region of said second conductivity type forming a drain for carriers of said second conductivity type in said portion of said relatively lightly doped region of said first conductivity type between said gates to create a deep-depletion region therein and provide enhanced forward

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blocking capability for the device when a voltage is applied to said gate electrode means to turn off the device.

2. The device of claim 1, further comprising a second region of said second conductivity type opposite to said first conductivity type formed in said wafer between said trenches and extending from said first semiconductor surface through said first relatively highly doped region of said first conductivity type and through at least a part of said relatively lightly doped region of said first conductivity type, said second region of said second conductivity type being spaced from said trenches on opposite sides thereof by said first relatively highly doped region of said first conductivity type and by said part of said relatively lightly doped region of said first conductivity type through which said second region of said second conductivity type extends;

whereby, when said voltage is applied to said gate electrode means to turn off the device, carriers of said first conductivity type generated in said portion of said relatively lightly doped region of said first conductivity type between said gates are depleted from said relatively lightly doped region of said first conductivity type between said gate electrode means by action of gate depletion and junction depletion to further enhance the forward blocking capability of the device.

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3. The device of claim 1, wherein:

said trenches each extend in a first longitudinal direction parallel to said first and second semiconductor surfaces;

said gate electrode means disposed in said trenches have respective longitudinal faces extending in said first longitudinal direction; and

said first region of said second conductivity type extends in a second longitudinal direction perpendicular to said first longitudinal direction.

4. The device of claim 3, wherein:

said trenches each extend in a first longitudinal direction parallel to said first and second semiconductor surfaces;

said gate electrode means disposed in said trenches have respective longitudinal faces extending in said first longitudinal direction;

said first region of said second conductivity type extends in a second longitudinal direction perpendicular to said first longitudinal direction; and

said second region of said second conductivity type extends longitudinally in said first longitudinal direction.

5. A high power metal oxide semiconductor field effect trench transistor device exhibiting relatively low on-resistance and relatively high breakdown voltage, said device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces, said wafer of

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semiconductor material including a relatively lightly doped region of a first conductivity type, a plurality of spaced narrow trenches formed perpendicularly in said wafer and extending from said first semiconductor surface, at least a portion of said relatively lightly doped region being disposed between said trenches;

gate electrode means disposed in said trenches and spaced from said portion of said relatively lightly doped region by a layer of gate insulation material;

a first relatively highly doped region of said first conductivity type disposed between and adjacent to said first semiconductor surface and said relatively lightly doped region; and

a first region of a second conductivity type opposite to said first conductivity type formed in said wafer between said trenches and extending from said first semiconductor surface through said first relatively highly doped region of said first conductivity type and through at least a part of said relatively lightly doped region of said first conductivity type, said first region of said second conductivity type being spaced from said trenches on opposing sides thereof by said first relatively highly doped region of said first conductivity type and by said part of said relatively lightly doped region of said first conductivity type through which said first region of said second conductivity type extends, said first region of a second conductivity type depleting carriers of said first conductivity type from said relatively lightly doped region of said first conductivity type between said gates by action of gate depletion and junction depletion to provide enhanced

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forward blocking capability for the device when a voltage is applied to said gate electrode means to turn off the device.

6. The device of claim 5, wherein:

said trenches each extend in a first longitudinal direction parallel to said first and second semiconductor surfaces;

said gate electrode means disposed in said trenches have respective longitudinal faces extending in said first longitudinal direction; and

said first region of said second conductivity type extends longitudinally in said first longitudinal direction.

7. The device of claim 1, 2, or 5 wherein said relatively lightly doped region of said first conductivity type extends beneath and laterally under said trenches.

8. The device of claim 1, 2, or 5 further comprising a second relatively highly doped region of said first conductivity type disposed between and adjacent to said second semiconductor surface and said relatively lightly doped region of said first conductivity type.

9. The device of claim 8, wherein said second relatively highly doped region of said first conductivity type extends upwardly from said second semiconductor surface and between said trenches.

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10. The device of claim 1, 2, or 5 further comprising a first relatively highly doped region of said second conductivity type disposed between and adjacent to said second semiconductor surface and said relatively lightly doped region of said first conductivity type.

11. The device of claim 1, 2, or 5 wherein said device is provided in a cellular topology comprising a plurality of parallel-connected polygonal cells.

12. A high power metal oxide semiconductor field effect trench transistor device exhibiting relatively low on-resistance and relatively high breakdown voltage, said device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces;

a relatively lightly doped region of a first conductivity type formed in said wafer and extending from said first semiconductor surface to a substrate portion of said wafer, said substrate portion comprising a region of a second conductivity type;

gate insulation means on said first semiconductor surface and disposed at least on said relatively lightly doped region of said first conductivity type;

gate electrode means disposed over said gate insulation means;

a relatively highly doped drain region of said first conductivity type formed in said wafer and extending from said first semiconductor surface to said substrate portion of said wafer, said drain region being

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disposed laterally and adjacent to said relatively lightly doped region of said first conductivity on a first side thereof;

a relatively highly doped source region of said first conductivity type formed in said wafer and extending from said first semiconductor surface to said substrate portion of said wafer, said source region being disposed laterally and adjacent to said relatively lightly doped region of said first conductivity on a second side thereof opposite to said first side; and

a first region of a second conductivity type opposite to said first conductivity type, said first region of said second conductivity type being formed in said wafer and extending from said first semiconductor surface adjacent to and at least partially co-extensive with said first relatively highly doped source region of said first conductivity type;

whereby, when a voltage having the same polarity as said first conductivity type is applied to said gate electrode means, said first region of said second conductivity type forms a drain for carriers of said second conductivity type in said portion of said relatively lightly doped region of said first conductivity type under said gate electrode means to create a deep-depletion region therein and provide enhanced forward blocking capability for the device.

13. The device of claim 1, 2, 5, or 12 wherein said first conductivity type comprises N-type and said second conductivity type comprises P-type.

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