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CONTROL CIRCUIT FOR SOLID-STATE SWITCHES

This invention relates to control circuits for controlling solid-state switches, in particular for
5 controlling the state of solid-state switches which have high voltage and relatively high current capabilities.

U.S. Patent 4,250,409 describes control circuitry for controlling the state of high voltage and relatively high current capability solid-state switches such as the
10 gated diode switches (GDS's) described in the article entitled "A 500 V Monolithic Bidirectional 2 x 2 Crosspoint Array," 1980 IEEE International Solid-State Circuits Conference-Digest of Technical Papers pages 170 and 171. As the patent points out, special problems in
15 controlling the GDS result from the need to provide or to remove a large current from the gate to switch the device to the OFF state. The control circuitry consists of a moderate number of transistors and a current limiter element. One problem with this control circuitry is that
20 somewhat undesirable current levels are injected into the load switches and the circuits associated therewith because of variations in the current limiter.

It is desirable to have circuitry which performs the same basic function as the above-described control
25 circuitry but which does not require a current limiter and which requires fewer components and less silicon area for implementation.

28 According to this invention there is provided a

control circuit for use with a first gated diode switching device of the type comprising a semiconductor body having a bulk portion of relatively high resistivity, a first region of a first conductivity type and of relatively low resistivity, and second and third regions of a second conductivity type opposite that of the first conductivity type, the first and third regions being connected to output terminals of the device, the second region being coupled to a control terminal of the device, and the first, second and third regions being mutually separated by portions of the bulk of the semiconductor body, including a second gated diode switching device of the same type and essentially same electrical characteristics as the first device and having an output terminal coupled to the control terminal of the first device, the control circuit being capable of supplying up to a preselected level of current into the second device, and third and fourth switching devices each having a control terminal and first and second output terminals, the control terminal of the third device and a first output terminal of the fourth device being coupled to a first control circuit input terminal, a second output terminal of the fourth device being coupled to a first output terminal of the second device, the control terminal of the fourth device and the first output terminal of the third device being coupled to a second control circuit terminal, and a second output terminal of the third device being coupled to the control terminal of the second device.

The invention will now be described by way of example with reference to the accompanying drawing which illustrates a switching system embodying the invention.

Referring now to the drawing a switching system 10 comprises control circuitry 12 (within the largest line rectangle) which is coupled by an output terminal 34 to the gates of a pair of high voltage load (pass) gated diode switching devices GDSL1 and GDSL2. The anode 38 of GDSL1 and the cathode of GDSL2 are coupled to a

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terminal X0 and to a first terminal of a resistor R3. A second terminal of R3 is coupled to a terminal 36 and to a potential source V1. The anode of GDSL2 and the cathode of GDSL1 are coupled to a terminal Y0 and to a first terminal of a resistor R4. A second terminal of R4 is coupled to a terminal 38 and to a potential source V2. The combination of GDSL1 and GDSL2 functions as a bidirectional switch which selectively conducts between terminals X0 and Y0 via a relatively low resistance path through GDSL1 or GDSL2. Control circuitry 12 functions so as to supply the needed potentials at terminals 34 and X0 and to supply the needed potentials and current sourcing or sinking capability necessary to control the states of GDSL1 and GDSL2.

As is known, a gated diode switch (GDS) comprises a semiconductor body having a bulk portion which is of a first conductivity type and a relatively high resistivity, an anode region of the first conductivity type and of a relatively low resistivity, gate and cathode regions of a second conductivity type opposite that of the first conductivity type. The anode and cathode regions are connected to output terminals of the switch. The gate region is connected to a control terminal of the switch. The anode, gate, and cathode regions are mutually separated by portions of the bulk of the semiconductor body. Conduction during the ON state between the cathode and anode regions is by dual carrier injection which forms a conductive plasma. The device is turned to the OFF state by applying a sufficient voltage to the gate region to deplete the bulk portion between the anode and cathode regions of carriers.

Control circuitry 12 essentially comprises a high voltage switch GDSC, a first voltage branch circuit 14 (illustrated within a dashed line rectangle), and a second voltage branch circuitry 16 (illustrated within another dashed line rectangle). For illustrative purposes, GDSC is assumed to be a gated diode switch. Branch circuit 14 selectively maintains GDSL1 and GDSL2 in the ON state

such that conduction can occur through one or the other GDSL if the potentials of the anode and cathode terminals thereof are sufficient to support conduction, or it can inhibit conduction through both load switches by
5 maintaining the load switches in the OFF state, or it can, for relatively low current flow through GDSL1 and/or GDSL2, cause an interruption of said current flow (switch one of the GDSL's to the OFF state). Branch circuit 16 serves essentially to switch GDSL1 and GDSL2 OFF and,
10 therefore, helps interrupt (cut off) relatively large current flow between terminals X0 and Y0 independent of the potentials applied thereto so long as these potentials are within preselected limits.

Branch circuit 14 comprises p-n-p transistors Q1, .
15 Q2, and Q3, n-p-n transistor Q4, and resistors R1 and R2. A Vin input terminal 18 is coupled to a first terminal of R1. A second terminal of R1 is coupled to the bases of Q1 and Q2, the emitter of Q3, and to a terminal 20. The emitter of Q1 is coupled to a first terminal of R2 and
20 to a terminal 22. A second terminal of R2 is coupled to the emitter of Q2, the base of Q3, and to a terminal 26 which is coupled to a power supply V++. The collector of Q1 is coupled to the base of Q4 and to a terminal 24. The collector of Q2 is coupled to the gate of GDSC and to a
25 terminal 28. The collector of Q3 is coupled to the anode of GDSC and to a terminal 30. The emitter of Q4 is coupled to X0, and the collector of Q4 is coupled to the gates of GDSL1 and GDSL2, the cathode of GDSC, and to output terminal 34.

30 Branch circuit 16 comprises essentially a diode D1 whose cathode is connected to terminal 30 and whose anode is coupled to a terminal 32 and to a power supply V+. Typically, power supply V+ is less positive in potential than power supply V++.

35 The basic operation of system 10 is as follows:
Assuming that GDSL1 and GDSL2 are not conducting and the voltage applied to input terminal 18 is a "1" (which is
38 typically 2.5 volts more positive than V++), then Q1, Q2,

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and Q4 are biased OFF, and Q3 is biased ON. GDSC is biased ON since the anode thereof (terminal 30) is at a potential close to V++, and the gate terminal is typically floating in potential at the level of V++ or a less positive level. Leakage currents of GDSL1 and GDSL2 can flow from terminal 18 through the emitter-collector of Q3, through the anode-cathode of GDSC, and into the gates of GDSL1 and GDSL2. Approximately the potential level of V++ appears at terminal 34. GDSL1 and GDSL2 are biased OFF and are inhibited from conducting current.

Now assuming that Vin switches from a "1" to "0" (a "0" voltage level being typically 2.2 volts less positive than V++), Q1, Q2, and Q4 are now biased ON, and Q3 is biased OFF. As Q2 becomes biased ON, the potential of the gate of GDSC (terminal 28) increases to approximately V++. The potential of the anode of GDSC (terminal 30), which had been also at approximately V++, starts to drop since GDSC and Q4 are both ON. The potentials of the anode and cathode of GDSC drop until they are approximately 20 volts below the potential of the gate of GDSC and then GDSC turns OFF. Then, since Q4 is ON, terminal 34 continues to move towards the potential of terminal X0.

Assume now that V1 is at +200 volts and V2 is at ground potential and that V++ = +315 volts and V+ = +275 volts. As terminal 34 moves to within approximately +20 volts of the potential of terminal X0, GDSL1 turns on and then rapidly causes terminal 34 to move to approximately the potential of terminal X0. Thus GDSL1 is ON and conducts current from terminal X0 to terminal Y0. Alternatively, if the potential of V2 were -200 and the potential of V1 becomes ground, then GDSL2 turns ON and conducts current from terminal Y0 to terminal X0.

Now, with current flowing through either GDSL1 or GDSL2, assume Vin is switched from a "0" to a "1". Q1, Q2, and Q4 are now switched OFF, and Q3 is switched ON. Initially the gate of GDSC (terminal 28) is at

approximately V_{++} , and the anode (terminal 30) is at about 20 volts lower potential. This results in GDSC being in the OFF state. The anode of GDSC then starts to increase in potential towards V_{++} and GDSC turns ON.

5 The anode, cathode, and gate potentials of GDSC now start to drop as current is sourced into the ON and conducting load gated diode switch (GDSL1 or GDSL2). The gate (terminal 28) of GDSC is held at approximately 0.7 volt below the anode (terminal 30) of GDSC since GDSC
10 is conducting. As the anode of GDSC drops in potential approximately one diode drop below the potential level of V_+ , D1 becomes conductive and supplies substantial current through GDSC and into terminal 34 and the gate of GDSL1 or GDSL2.

15 The potential of V_+ (terminal 32) and the current being supplied into the gate of GDSL1 or GDSL2 are both preselected to be sufficient to break current flow through the conducting gated diode load switch and thus to turn same OFF. As GDSL1 or GDSL2 turns OFF, the current flowing
20 into the gate thereof is significantly reduced. This allows terminal 30 to rise in potential to approximately the level of V_{++} and thus reverse biases D1. This cuts off all current flow from V_+ .

If the level of current flowing through GDSL1 or
25 GDSL2 is sufficiently low, then the relatively modest current flow through Q3 and into GDSC is sufficient to interrupt current flow through GDSL1 or GDSL2, and terminal 30 does not drop sufficiently in potential to forward bias D1.

30 The combination of transistors Q2 and Q3 controls GDSC and at least partly controls the state of GDSL1 and GDSL2, relatively independent of V_+ and D1 and the combination of Q1 and Q4, which are equivalent to corresponding transistors of U.S. Patent 4,250,409.

35 R3 and R4 serve to limit current which can flow through GDSL1 and/or GDSL2 and to allow for the potential difference between terminals X0 and Y0 to be typically
38 about 2.2 volts when GDSL1 or GDSL2 is ON and conducting.

Switching system 10 has been fabricated, tested, and found to be fully functional. Control circuitry 12 and GDSL1 and GDSL2 were all fabricated on a single semiconductor substrate using dielectric isolation. The circuitry fabricated also included a second pair of load gated diode switches with two additional transistors like Q1 and Q4. The cathode of GDSC of this fabricated circuitry was coupled to the anodes of a pair of additional diodes (not illustrated) which are similar to corresponding diodes illustrated in FIG. 4 of U.S. Patent 4,250,409.

In the circuitry fabricated $V_{++} = +315$ volts, $V_{+} = +275$ volts, $V_1 = +200$ volts, $V_2 = +200$ volts, $R_1 = 18k$ ohms, $R_2 = 10k$ ohms, $V_{in} "1" = +317.5$ volts, $V_{in} "0" = +312.8$ volts, and GDSC, GDSL1, and GDSL2, all had the basic structure disclosed in the article entitled "A 500 V Monolithic Bidirectional 2 x 2 Crosspoint Array," 1980 IEEE International Solid-State Circuits Conference-Digest of Technical Papers, pages 170 and 171.

The embodiments described herein are by way of example. Various modifications are possible. For example, bipolar transistors Q1, Q2, Q3, and Q4 could be field effect transistors or other types of switching devices which can handle relatively high voltages and moderate currents. A transistor or other switching device can be substituted for D1. Still further, electrically or optically activated switches, as are illustrated in FIG. 4 of U.S. Patent 4,250,409, can be inserted between D1 and power supply V_{+} . Still further, with approximate leakages for GDSC and GDSL1 and/or GDSL2, R2, Q1, and Q4 could be eliminated, and circuitry 14 would still be functional. Still further, a current limiter or like means could be coupled between terminal 34 and terminals X0 or Y0 or to a negative power supply and R2, Q1 and Q4 could be eliminated.

CLAIMS

1. A control circuit for use with a first gated diode switching device of the type comprising a semiconductor body having a bulk portion of relatively high resistivity, a first region of a first conductivity type and of relatively low resistivity, and second and third regions of a second conductivity type opposite that of the first conductivity type, the first and third regions being connected to output terminals of the device, the second region being coupled to a control terminal of the device, and the first, second and third regions being mutually separated by portions of the bulk of the semiconductor body, including a second gated diode switching device of the same type and essentially same electrical characteristics as the first device and having an output terminal coupled to the control terminal of the first device, the control circuit being capable of supplying up to a preselected level of current into the second device, and third and fourth switching devices each having a control terminal and first and second output terminals, the control terminal of the third device and a first output terminal of the fourth device being coupled to a first control circuit input terminal, a second output terminal of the fourth device being coupled to a first output terminal of the second device, the control terminal of the fourth device and the first output terminal of the third device being coupled to a second control circuit terminal, and a second output terminal of the third device being coupled to the control terminal of the second device.

2. A circuit as claimed in claim 1 including a branch circuit coupled to the second device for supplying into the second device a substantially greater level of current than the preselected level, if, and only if, the level of current flow into the second device reaches the preselected level, and fifth and sixth switching devices each having a control terminal and first and second output terminals and being capable of relatively high voltage



operation, the control terminal, the second output terminal, and the first output terminal of the fifth device being coupled to the control terminal of the third device, the control terminal of the sixth device, and
5 the control terminal of the fourth device, respectively, and the first and second output terminals of the sixth device being coupled to one of the output terminals of the first device and the second output terminal of the second switching device, respectively.

10 3. A circuit as claimed in claim 2 including first and second resistance means each having a first and second terminal, the first terminal of the first resistance means being coupled to the first control circuit input terminal, the second terminal of the first resistance
15 means being coupled to the control terminals of the third and fifth devices and to the first output terminal of the fourth device, the first terminal of the second resistance means being coupled to the first output terminal of the fifth device, and the second terminal of
20 the second resistance means being coupled to the first output terminal of the third device and to the control terminal of the fourth device.

4. A circuit as claimed in claim 3 wherein the first and second devices are structurally adapted for
25 high voltage and relatively high current operation, the third, fourth, fifth, and sixth switching devices are structurally adapted for high voltage and modest current operation, and the first and second resistance means are first and second resistors.

30 5. A control circuit substantially as herein described with reference to the accompanying drawing.
